STIC Search Report
EIC 2100

STIC Database Tracking Number: 116921

TO: John Lane **Location:** **Art Unit : 2188** **Tuesday, March 23, 2004** **Case Serial Number: 09/973279**	**From: Terese Esterheld** **Location: EIC 2100** **PK2-4B30** **Phone: 308-7795** **Terese.esterheld@uspto.gov**

Search Notes

Dear Examiner Lane,

Attached, please find the results of your search request for application 09/973279. I have concentrated on finding information on Translation lookaside buffer?, Context,and Validate.

Please look over the complete set as items not marked may also be of value to you.

Please let me if you need additional information on this search.

Thank you for coming to EIC 2100.

Terese Esterheld

Access DB# 116921 (83)

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: jack lane_____ Examiner # :68699____ Date: 03/15/04___
Art Unit: _2188_____ Phone Number 305-3818_ Serial Number: _09/973,279____
Mail Box Location: __2Y13____ Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: __Method and Device for a Context-based Memory Management System_____

Inventors (please provide full names): __Boris Ostrovksy, Pazhani Pillai, Daniel R. Cassiday, Christopher J. Jackson, John R. Feehrer, Mark Donald Hill, David A. Wood_____

Earliest Priority Filing Date: _10/09/2001_____

***For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.**

See Abstract and claims

Search:
Translat$ or tlb or map$4
Context
Valid$

****

STAFF USE ONLY

Searcher: Terese Estenfeld
Searcher Phone #: 308-7795
Searcher Location: 4B 30
Date Searcher Picked Up: 3/22/04 11:30am
Date Completed: 3/23/04 10:00am
Searcher Prep & Review Time: _____
Clerical Prep Time: _____

Type of Search

NA Sequence (#)_____
AA Sequence (#)_____
Structure (#) _____
Bibliographic _____
Litigation _____
Fulltext _____
Patent Family _____

Vendors and cost where applicable

STN _____
Dialog _____
Questel/Orbit _____
Dr.Link _____
Lexis/Nexis _____
Sequence Systems _____
WWW/Internet _____

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Set     Items   Description
S1       1470   AU=(OSTROVSKY, B? OR OSTROVSKY B? OR CASSIDAY, D? OR CASSI-
            DAY D? OR FEEHRER, J? OR FEEHRER J? OR WOOD, D? OR WOOD D? OR
            PILLAI, P? OR PILLAI P? OR JACKSON, C? OR JACKSON C? OR HILL,
            M? OR HILL M?)
S2        224   S1 AND IC=G06F?
S3         85   S2 AND IC=(G06F-012? OR G06F-009?)
S4         52   S3 AND IC=(G06F-012/00 OR G06F-012/02 OR G06F-012/04 OR G0-
            6F-012/08 OR G06F-012/10 OR G06F-009/26 OR G06F-009/34)
File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)
        (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Mar W02
        (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040318,UT=20040311
        (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200419
        (c) 2004  Thomson Derwent
```

4/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

06061773 **Image available**
DATA REPLACING METHOD IN COMPUTER SYSTEM

PUB. NO.: 11-003280 [JP 11003280 A]
PUBLISHED: January 06, 1999 (19990106)
INVENTOR(s): HAGERSTEN ERIK E
HILL MARK D
APPLICANT(s): SUN MICROSYST INC
APPL. NO.: 09-184599 [JP 97184599]
FILED: June 26, 1997 (19970626)
PRIORITY: 674560 [US 674560], US (United States of America), July 01, 1996 (19960701)
INTL CLASS: **G06F-012/08 ; G06F-012/08 ; G06F-015/163**

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method to decide a write-back protocol that is most suitable for every memory level by adding a copy-back cache of a low level and a write-through cache of a high level to a memory hierarchy of a skip level.
SOLUTION: The COMA node memories 114 to 184 are placed distant from the L3$ 118 to 188, and each of processors 111a to 181i includes an internal cache (L1$) of a 1st level. Therefore, the cache memory hierarchy of a computer system 100 includes L1$, L2$, L3$ and a separate COMA cache. When the data are cached in a COMA mode, the inclusion is maintained between the L1$ and L2$ and also between the L2$ and COMA cache. Thus, the L3$ is not used. When the data are cached in a NUMA mode, the memory 114 is not used. As a result, a hybrid NUMA/COMA architecture has no inclusion between the L2$ and COMA cache.

4/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05931129 **Image available**
METHOD FOR SELECTING DATA TO BE CACHED IN COMPUTER SYSTEM, COMPUTER SYSTEM AND CACHING DEVICE FOR COMPUTER SYSTEM

PUB. NO.: 10-214229 [JP 10214229 A]
PUBLISHED: August 11, 1998 (19980811)
INVENTOR(s): HAGERSTEN ERIK E
HILL MARK D
APPLICANT(s): SUN MICROSYST INC [198211] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 09-184600 [JP 97184600]
FILED: June 26, 1997 (19970626)
PRIORITY: 7-675,306 [US 675306-1996], US (United States of America), July 01, 1996 (19960701)
INTL CLASS: [6] **G06F-012/08 ; G06F-015/163**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)

4/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05931124 **Image available**
EFFECTIVE SELECTION FOR MEMORY STORAGE MODE IN COMPUTER SYSTEM

PUB. NO.: 10-214224 [JP 10214224 A]
PUBLISHED: August 11, 1998 (19980811)
INVENTOR(s): HAGERSTEN ERIK E
HILL MARK D
APPLICANT(s): SUN MICROSYST INC [198211] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 09-186076 [JP 97186076]
FILED: June 27, 1997 (19970627)
PRIORITY: 7-674,029 [US 674029-1996], US (United States of America), July 01, 1996 (19960701)
INTL CLASS: [6] **G06F-012/08**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

4/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05904531 **Image available**
EXTENDED SYMMETRICAL MULTIPROCESSOR ARCHITECTURE

PUB. NO.: 10-187631 [JP 10187631 A]
PUBLISHED: July 21, 1998 (19980721)
INVENTOR(s): HAGERSTEN ERIK E
HILL MARK D
SINGHAL ASHOK
APPLICANT(s): SUN MICROSYST INC [198211] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 09-211430 [JP 97211430]
FILED: July 02, 1997 (19970702)
PRIORITY: 7-675,361 [US 675361-1996], US (United States of America), July 02, 1996 (19960702)
7-675,362 [US 675362-1996], US (United States of America), July 02, 1996 (19960702)
7-675,363 [US 675363-1996], US (United States of America), July 02, 1996 (19960702)
INTL CLASS: [6] **G06F-015/16 ; G06F-012/08 ; G06F-012/08 ; G06F-013/36 ; G06F-015/163**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

4/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05904427 **Image available**
DEVICE AND METHOD FOR PREVENTING ACCESS CONTENTION

PUB. NO.: 10-187527 [JP 10187527 A]
PUBLISHED: July 21, 1998 (19980721)
INVENTOR(s): HAGERSTEN ERIK E
HILL MARK DONALD
APPLICANT(s): SUN MICROSYST INC [198211] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 09-187269 [JP 97187269]
FILED: June 30, 1997 (19970630)
PRIORITY: 7-673,130 [US 673130-1996], US (United States of America), July 01, 1996 (19960701)
INTL CLASS: [6] **G06F-012/00 ; G06F-009/46**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

4/5/6 (Item 6 from file: 347)

DIALOG(R)File 347:JAPIO
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05860383 **Image available**
MULTIPROCESS SYSTEM CONSTITUTED SO AS TO DETECT AND EFFICIENTLY PROVIDE MIGRATORY DATA ACCESS PATTERN

PUB. NO.: 10-143483 [JP 10143483 A]
PUBLISHED: May 29, 1998 (19980529)
INVENTOR(s): HAGERSTEN ERIK E
HILL MARK D
APPLICANT(s): SUN MICROSYST INC [198211] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 09-208225 [JP 97208225]
FILED: June 30, 1997 (19970630)
PRIORITY: 7-674,330 [US 674330-1996], US (United States of America), July 01, 1996 (19960701)
INTL CLASS: [6] **G06F-015/16 ; G06F-012/08**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.2 (INFORMATION PROCESSING -- Memory Units)

4/5/7 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01037054
MULTIPROCESSING COMPUTER SYSTEM EMPLOYING A CLUSTER PROTECTION MECHANISM
MEHRPROZESSORRECHNERSYSTEM MIT VERWENDUNG EINES GRUPPENSCHUTZMECHANISMUS
SYSTEME DE MULTITRAITEMENT COMPRENANT DES MECANISMES DE PROTECTION DE GRAPPES
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
HAGERSTEN, Erik, 3451 Cork Oak Way, Palo Alto, CA 94303, (US)
JACKSON, Christopher, J. , 2 Mamie Lane, Westford, MA 01886-3042, (US)
NESHEIM, William, A., 8 Lowell Road, Windham, NH 03087, (US)
GUZOVSKIY, Aleksandr, 130 Bowden Street 210, Lowell, MA 01852, (US)
NGUYEN, Hien, Apartment 1 282 Grove Street, Auburndale, MA 02166, (US
LEGAL REPRESENTATIVE:
Harris, Ian Richard (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1010090 A1 000621 (Basic)
EP 1010090 B1 030813
WO 99012102 990311
APPLICATION (CC, No, Date): EP 98946854 980904; WO 98US18466 980904
PRIORITY (CC, No, Date): US 924385 970905
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: **G06F-015/00 ; G06F-012/10**
CITED PATENTS (EP B): EP 288636 A; DE 4034444 A
CITED PATENTS (WO A): EP 288636 A ; DE 4034444 A
CITED REFERENCES (EP B):
The VIC 8352F User's Manual version 1.1, 30-06-1994, Creative Electronics Systems, Petit-Lancy;
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	000621 A1	Published application with search report
Application:	990602 A1	International application (Art. 158(1))
Lapse:	040317 B1	Date of lapse of European Patent in a contracting state (Country, date): FI 20030813,
Assignee:	030423 A1	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US

Examination: 000621 A1 Date of request for examination: 20000306
Change: 020904 A1 International Patent Classification changed: 20020716
Change: 020904 A1 Title of invention (French) changed: 20020716
Grant: 030813 B1 Granted patent
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200333	857
CLAIMS B	(German)	200333	854
CLAIMS B	(French)	200333	1006
SPEC B	(English)	200333	14475
Total word count - document A			0
Total word count - document B			17192
Total word count - documents A + B			17192

4/5/8 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01036664
LOOK-UP TABLE AND METHOD OF STORING DATA THEREIN
NACHSCHLAGTABELLE UND VERFAHREN ZUR DATENSPEICHERUNG DARIN
TABLE DE CONSULTATION ET PROCEDE POUR Y ENREGISTRER DES DONNEES
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
HAGERSTEN, Erik, E., 3451 Cork Oak Way, Palo Alto, CA 94303, (US)
HILL, Mark , 272 Covington Road, Los Altos, CA 94024, (US
LEGAL REPRESENTATIVE:
Harris, Ian Richard (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1019840 A2 000719 (Basic)
EP 1019840 B1 031119
WO 99012103 990311
APPLICATION (CC, No, Date): EP 98944751 980904; WO 98US18469 980904
PRIORITY (CC, No, Date): US 924385 970905
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: **G06F-012/10 ; G06F-012/08 ; G06F-012/12**
CITED PATENTS (EP B): EP 780769 A; WO 98/29986 A
CITED PATENTS (WO A): XP 398997 ; XP 463373
CITED REFERENCES (EP B):
AGARWAL A ET AL: "COLUMN-ASSOCIATIVE CACHES: A TECHNIQUE FOR REDUCING THE MISS RATE OF DIRECT-MAPPED CACHES" PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, SAN DIEGO, MAY 16 - 19, 1993, no. SYMP. 20, 16 May 1993, pages 179-190, XP000398997 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
SEZNEC A: "ABOUT SET AND SKEWED ASSOCIATIVITY ON SECOND-LEVEL CACHES" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, CAMBRIDGE, MA., OCT. 3 - 6, 1993,3 October 1993, pages 40-43, XP000463373 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS;
CITED REFERENCES (WO A):
AGARWAL A ET AL: "COLUMN-ASSOCIATIVE CACHES: A TECHNIQUE FOR REDUCING THE MISS RATE OF DIRECT-MAPPED CACHES" PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, SAN DIEGO, MAY 16 - 19, 1993, no. SYMP. 20, 16 May 1993, pages 179-190, XP000398997 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
SEZNEC A: "ABOUT SET AND SKEWED ASSOCIATIVITY ON SECOND-LEVEL CACHES" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, CAMBRIDGE, MA., OCT. 3 - 6, 1993,3 October 1993, pages 40-43, XP000463373 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS;
NOTE:

No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	000719	A2	Published application without search report
Application:	990602	A2	International application (Art. 158(1))
Grant:	031119	B1	Granted patent
Change:	020918	A2	Title of invention (French) changed: 20020731
Change:	020918	A2	Title of invention (English) changed: 20020731
Change:	020918	A2	Title of invention (German) changed: 20020731
Change:	020918	A2	International Patent Classification changed: 20020731
Examination:	000719	A2	Date of request for examination: 20000306
Change:	020904	A2	International Patent Classification changed: 20020716
Change:	020904	A2	Title of invention (German) changed: 20020716
Change:	020904	A2	Title of invention (English) changed: 20020716
Change:	020904	A2	Title of invention (French) changed: 20020716
Assignee:	030423	A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200347	1114
CLAIMS B	(German)	200347	1128
CLAIMS B	(French)	200347	1202
SPEC B	(English)	200347	17165
Total word count - document A			0
Total word count - document B			20609
Total word count - documents A + B			20609

4/5/9 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00896601
Hybrid memory access protocol in a distributed shared memory computer system
Hybrides Speicherzugangsprotokoll in einem Datenverarbeitungssystem mit verteiltem, gemeinsamem Speicher
Protocole hybride pour acces de memoire dans un systeme a memoire distribuee et partagee
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View, California 94043-1100, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, CA 94043, (US)
Hill, Mark Donald , 2124 Chamberlain Avenue, Madison, WI 53705, (US
LEGAL REPRESENTATIVE:
Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 818732 A2 980114 (Basic)
EP 818732 A3 990310
APPLICATION (CC, No, Date): EP 97304524 970625;
PRIORITY (CC, No, Date): US 673957 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**

ABSTRACT EP 818732 A2
A method, in a computer network having a first plurality of nodes coupled to a common network infrastructure and a distributed shared memory distributed among the first plurality of nodes, for servicing a memory access request by a first node of the first plurality of nodes. The memory access request pertains to a memory block of a memory module that has a home node different from the first node in the computer network. The home node has a partial directory cache that has fewer

directory cache entries than a total number of memory blocks in the memory module. The method includes the step of ascertaining whether the memory block is currently cached in the partial directory cache. If the memory block is currently cached in the partial directory cache, the first memory access request is serviced using a directorv protocol. If the memorv block is not currently cached in the partial directory cache, the first memory access request is serviced using a directory-less protocol. The directory states pertaining to copies of the memory block in the network nodes is cached in the partial directory cache when the memory access request generates a renewal point with respect to the directory states.

ABSTRACT WORD COUNT: 201

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	020410 A2	Date of dispatch of the first examination report: 20020219
Application:	980114 A2	Published application (A1with Search Report ;A2without Search Report)
Assignee:	030423 A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Search Report:	990310 A3	Separate publication of the European or International search report
Examination:	991013 A2	Date of request for examination: 19990818

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9803	1994
SPEC A	(English)	9803	11297
Total word count - document A			13291
Total word count - document B			0
Total word count - documents A + B			13291

4/5/10 (Item 4 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00893826

Multi-level cache memory

Mehrstufiger Cachespeicher

Antememoire a plusieurs niveaux

PATENT ASSIGNEE:

SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View, California 94043-1100, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)

INVENTOR:

Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, California 94303, (US)

Hill, Mark D. , 272 Covington Road, Los Altos, California 94024, (US

LEGAL REPRESENTATIVE:

Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)

PATENT (CC, No, Kind, Date): EP 817080 A2 980107 (Basic)
EP 817080 A3 980121

APPLICATION (CC, No, Date): EP 97304726 970630;

PRIORITY (CC, No, Date): US 674029 960701

DESIGNATED STATES: DE; FR; GB; IT; NL; SE

INTERNATIONAL PATENT CLASS: **G06F-012/08**

ABSTRACT EP 817080 A3

An efficient scheme for selecting memory storage modes of a multi-level cache hierarchy of a computing system having at least a lower-level cache (LLC) and a higher-level cache (HLC). In one embodiment, memory space in the lower-level cache (LLC) is allocated in cache-line sized units, while memory space in the higher-level cache (HLC) is allocated in page sized units; with each page including two or more cache lines. Accordingly, during the execution of a program. cache-line-sized components of a page-sized block of data are incrementally stored in the cache lines of

the LLCs. Subsequently, the system determines that it is time to review the allocation of cache resources, i.e., between the LLC and the HLC. The review trigger may be external to the processor, e.g., a timer interrupting the processor on a periodic basis. Alternatively, the review trigger may be from the LLC or the HLC, e.g., when the LLC is full, or when usage of the HLC drops below a certain percentage. A review of the allocation involves identifying components associated with their respective blocks of data and determining if the number of cached components identified with the blocks exceed a threshold. If the threshold is exceeded for cached components associated with a particular block, space is allocated in the HLC for storing components from the block. This scheme advantageously increases the likelihood of future cache hits by optimally using the HLC to store blocks of memory with a substantial number of useful components.

ABSTRACT WORD COUNT: 246

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	001122 A2	Date of dispatch of the first examination report: 20001010
Application:	980107 A2	Published application (A1with Search Report ;A2without Search Report)
Assignee:	030423 A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Search Report:	980121 A3	Separate publication of the European or International search report
Examination:	980805 A2	Date of filing of request for examination: 980604
Change:	980930 A2	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9802	797
SPEC A	(English)	9802	4023
Total word count - document A			4820
Total word count - document B			0
Total word count - documents A + B			4820

4/5/11 (Item 5 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00893825

Skip-level write-through in a multi-level memory of a computer system

Durchschreiboperation mit Stufenumgehung in einem mehrstufigen Speicher eines Rechnersystems

Operation d'ecriture au travers a contournement de niveaux dans une memoire a plusieurs niveaux d'un systeme d'ordinateur

PATENT ASSIGNEE:

Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)

INVENTOR:

Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, California 94303, (US)

Hill, Mark D. , 272 Covington Road, Los Altos, California 94024, (US

LEGAL REPRESENTATIVE:

Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)

PATENT (CC, No, Kind, Date): EP 817079 A2 980107 (Basic)
EP 817079 A3 980128
EP 817079 B1 030903

APPLICATION (CC, No, Date): EP 97304725 970630;

PRIORITY (CC, No, Date): US 674560 960701

DESIGNATED STATES: DE; FR; GB; IT; NL; SE

INTERNATIONAL PATENT CLASS: **G06F-012/08**

CITED PATENTS (EP B): EP 681241 A

CITED REFERENCES (EP B):

ANONYMOUS: "Second Level Cache for MP Systems" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 1A, June 1984, NEW YORK, US, pages 298-300, XP002048711
JOE T ET AL: "EVALUATING THE MEMORZ OVERHEAD REQUIRED FOR COMA ARCHITECTURES" PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, CHICAGO, APRIL 18 - 21, 1994, no. SYMP. 21, 18 April 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 82-93, XP000480427;

ABSTRACT EP 817079 A3

A flexible scheme is provided for designating the appropriate write-back protocol best suited for each memory level within a multi-level-cache computer system. The skip-level memory hierarchy of the present invention includes a lower-level copy-back cache and a higher-level write-through cache. This greatly simplifies the implementation of the higher-level cache, since it may be implemented with a write-or-read access to its address tag. Although counterintuitive, a write-through higher-level cache in a distributed shared memory may also increase the efficiency of the computer system without unduly increasing the volume of network traffic within the computer system. This is because a write-through higher-level cache increases the probability of readily-available cached copies of updated data which are consistent with the home copies of the data, thereby reducing the number of fetches from remote home locations whenever the data is not found in the lower-level cache but is found in the higher-level cache.

ABSTRACT WORD COUNT: 149

NOTE:
Figure number on first page: 1A

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	001206 A2	Date of dispatch of the first examination report: 20001018
Application:	980107 A2	Published application (A1with Search Report ;A2without Search Report)
Grant:	030903 B1	Granted patent
Assignee:	030423 A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Search Report:	980128 A3	Separate publication of the European or International search report
Examination:	980805 A2	Date of filing of request for examination: 980608
Change:	981007 A2	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199802	384
CLAIMS B	(English)	200336	806
CLAIMS B	(German)	200336	794
CLAIMS B	(French)	200336	1037
SPEC A	(English)	199802	3065
SPEC B	(English)	200336	3191
Total word count - document A			3450
Total word count - document B			5828
Total word count - documents A + B			9278

4/5/12 (Item 6 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00893823

Allocation of cache memory space in a computer system
Cachespeicherbereich-Zuordnung in einem Rechnersystem
Allocation d'espace d'antememoire dans un systeme d'ordinateur

PATENT ASSIGNEE:

SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View, California 94043-1100, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)
INVENTOR:
Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, California 94303, (US)
Hill, Mark D. , 272 Covington Road, Los Altos, California 94024, (US
LEGAL REPRESENTATIVE:
Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 817078 A2 980107 (Basic)
EP 817078 A3 980121
APPLICATION (CC, No, Date): EP 97304723 970630;
PRIORITY (CC, No, Date): US 675306 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**
ABSTRACT EP 817078 A3

An efficient cache allocation scheme is provided for both uniprocessor and multiprocessor computer systems having at least one cache. In one embodiment, upon the detection of a cache miss, a determination of whether the cache miss is "avoidable" is made. In other words, would the present cache miss have occurred if the data had been cached previously and if the data had remained in the cache. One example of an avoidable cache miss in a multiprocessor system having a distributed memory architecture is an excess cache miss. An excess cache miss is either a capacity miss or a a conflict miss. A capacity miss is caused by the insufficient size of the cache. A conflict miss is caused by insufficient depth in the associativity of the cache. The determination of the excess cache miss involves tracking read and write requests for data by the various processors and storing some record of the read/write request history in a table or linked list. Data is cached only after an avoidable cache miss has occured. By caching only at least one avoidable cache miss instead of upon every (initial) access, cache space can be allocated in a highly efficient manner thereby minimizing the number of data fetches caused by cache misses.
ABSTRACT WORD COUNT: 209

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	001122 A2	Date of dispatch of the first examination report: 20001010
Application:	980107 A2	Published application (A1with Search Report ;A2without Search Report)
Assignee:	030423 A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Search Report:	980121 A3	Separate publication of the European or International search report
Examination:	980805 A2	Date of filing of request for examination: 980604
Change:	980930 A2	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9802	1135
SPEC A	(English)	9802	2883
Total word count - document A			4018
Total word count - document B			0
Total word count - documents A + B			4018

4/5/13 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00893746
A multiprocessing system configured to detect and efficiently provide for migratory data access patterns
Multiprozessorsystem ausgestaltet zur Erkennung und zum effizienten

Handhabung von Migrationsdatenzugriffsmustern
Systeme multiprocesseur congigure pour detecter et fournir efficacement des formes d'acces en memoire de donnee migratoire

PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, California 94303, (US)
Hill, Mark D. , 2124 Chamberlain Avenue, Madison, WI 53705, (US
LEGAL REPRESENTATIVE:
Harris, Ian Richard et al (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)

PATENT (CC, No, Kind, Date): EP 817071 A2 980107 (Basic)
EP 817071 A3 980805
EP 817071 B1 030917
APPLICATION (CC, No, Date): EP 97304615 970627;
PRIORITY (CC, No, Date): US 674330 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**
CITED PATENTS (EP B): EP 443755 A
CITED REFERENCES (EP B):
STENSTROM P ET AL: "AN ADAPTIVE CACHE COHERENCE PROTOCOL OPTIMIZED FOR MIGRATORY SHARING" COMPUTER ARCHITECTURE NEWS, vol. 21, no. 2, 1 May 1993, pages 109-118, XP000380359
COX A L ET AL: "ADAPTIVE CACHE COHERENCY FOR DETECTING MIGRATORY SHARED DATA" COMPUTER ARCHITECTURE NEWS, vol. 21, no. 2, 1 May 1993, pages 98-108, XP000380358
BLACK D L ET AL: "COMPETITIVE MANAGEMENT OF DISTRIBUTED SHARED MEMORY" INTELLECTUAL LEVERAGE, SAN FRANCISCO, FEB. 27 - MAR. 3, 1989, no. CONF. 34, 27 February 1989, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 184-190, XP000092718;

ABSTRACT EP 817071 A2
A computer system includes a directory at each node which stores coherency information for the coherency units for which that node is the home node. In addition, the directory stores a data access state corresponding to each coherency unit which indicates the data access pattern observed for that coherency unit. The data access state may indicate migratory or non-migratory data access patterns. If the coherency unit has been observed to have a migratory data access pattern, then read/write access rights are granted. Conversely, if the coherency unit has been observed to have non-migratory data access patterns, then read access rights are granted. The home node further detects the migratory and non-migratory data access patterns and selects transitions between the migratory and non-migratory data access states independent of the cache hierarchies within the nodes which access the affected coherency unit. In one embodiment, a pair of counters are employed for each coherency unit. One of the counters is incremented when the coherency unit is in the migratory data access state and a data migration is detected. The other counter is incremented when the coherency unit is in the non-migratory data access state and a data migration is detected. When one of the counters overflows, the home node transitions the data access state of the coherency unit to the alternate data access state.
ABSTRACT WORD COUNT: 222
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):
Examination: 000809 A2 Date of dispatch of the first examination report: 20000627
Application: 980107 A2 Published application (A1with Search Report ;A2without Search Report)
Grant: 030917 B1 Granted patent
Change: 021016 A2 Title of invention (French) changed: 20020829
Change: 021016 A2 Title of invention (German) changed: 20020829
Change: 020911 A2 Title of invention (German) changed: 20020725
Change: 020911 A2 Title of invention (French) changed: 20020725

Assignee:	030423 A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Search Report:	980805 A3	Separate publication of the European or International search report
Examination:	990210 A2	Date of filing of request for examination: 981215
Change:	990421 A2	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199802	1047
CLAIMS B	(English)	200338	1298
CLAIMS B	(German)	200338	1364
CLAIMS B	(French)	200338	1610
SPEC A	(English)	199802	16478
SPEC B	(English)	200338	16326
Total word count - document A			17527
Total word count - document B			20598
Total word count - documents A + B			38125

4/5/14 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00893686
Methods and apparatus for a coherence transformer with limited memory for connecting computer system coherence domains
Verfahren und Vorrichtung fur einen Koharenzumwandler mit begrenztem Speicher zur Verbindung von Rechnersystem-Koharenzdomanen
Procede et dispositif pour transformateur de coherence avec memoire limitee permettant la connexion des domaines de coherence de systeme d'ordinateur
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
Hagersten, Erik E, 3451 Cork Oak Way, Palo Alto CA 94043, (US)
Hill, Mark Donald , 2124 Chamberlain Avenue, Madison WI 53705, (US)
Wood, David A , 2115 Bascon Street, Madison WI 53705, (US
LEGAL REPRESENTATIVE:
Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 817069 A1 980107 (Basic)
EP 817069 B1 030502
APPLICATION (CC, No, Date): EP 97304526 970625;
PRIORITY (CC, No, Date): US 677014 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**
CITED PATENTS (EP B): US 5522058 A
CITED REFERENCES (EP B):
LOVETT T ET AL: "STING: A CC-NUMA COMPUTER SYSTEM FOR THE COMMERCIAL MARKETPLACE" COMPUTER ARCHITECTURE NEWS, vol. 24, no. 2, May 1996, pages 308-317, XP000592195
LENOSKI D ET AL: "THE STANFORD DASH MULTIPROCESSOR" COMPUTER, vol. 25, no. 3, March 1992, pages 63-79, XP000288291
O'KRAFKA B W ET AL: "AN EMPIRICAL EVALUATION OF TWO MEMORY-EFFICIENT DIRECTORY METHODS" PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, SEATTLE, MAY 28 - 31, 1990, no. SYMP. 17, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 138-147, XP000144792;

ABSTRACT EP 817069 A1
A coherence transformer for allowing a computer node and one or more external devices to share memory blocks having local physical addresses at a memory module of the computer node. The coherence transformer

includes logic for ascertaining whether a memory access request from the external device for a memory block should be responded to using a snoop-only approach or an Mtag-only approach. The snoop-only approach requires a tag in a snoop tag array of the coherence transformer be available to track the memory block for an entire duration that the memory block is cached by the external device. The Mtag-only approach only temporarily stores the memory block until a global state associated with the memory block can be written back into the memory module of the computer node. The snoop tag array allows the coherence transformer to snoop the bus of the computer node to intervene and respond to memory access requests pertaining to a memory block externally cached and tracked by the snoop tag array.

ABSTRACT WORD COUNT: 167

NOTE:
Figure number on first page: 7A

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	010117	A1	Date of dispatch of the first examination report: 20001127
Application:	980107	A1	Published application (A1with Search Report ;A2without Search Report)
Lapse:	040107	B1	Date of lapse of European Patent in a contracting state (Country, date): NL 20030502, SE 20030802,
Change:	030813	B1	Inventor information changed: 20030627
Assignee:	030423	A1	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Grant:	030502	B1	Granted patent
Lapse:	031210	B1	Date of lapse of European Patent in a contracting state (Country, date): SE 20030802,
Examination:	980722	A1	Date of filing of request for examination: 980520
Change:	980916	A1	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199802	2897
CLAIMS B	(English)	200318	2473
CLAIMS B	(German)	200318	2215
CLAIMS B	(French)	200318	3036
SPEC A	(English)	199802	17512
SPEC B	(English)	200318	16881
Total word count - document A			20412
Total word count - document B			24605
Total word count - documents A + B			45017

4/5/15 (Item 9 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00893685

Methods and apparatus for substantially memory-less coherence transformer for connecting computer node coherence domains

Verfahren und Vorrichtung fur einen im wesentlichen speicherlosen Koharenzumwandler zur Verbindung von Rechnerknoten-Koharenzdomanen

Procede et dispositif pour transformateur de coherence essentiellement sans memoire permettant la connexion des domaines de coherence de noeud d'ordinateur

PATENT ASSIGNEE:

SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View, California 94043-1100, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)

INVENTOR:

Hagersten,Erik E, 3451 Cork Oak Way, Palo Alto CA 94043, (US)

Hill, Mark Donald , 2124 Chamberlain Avenue, Madison WI 53705, (US)
Wood,David A , 2115 Bascon Street, Madison WI 53705, (US
LEGAL REPRESENTATIVE:
Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 817068 A1 980107 (Basic)
APPLICATION (CC, No, Date): EP 97304525 970625;
PRIORITY (CC, No, Date): US 677012 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**

ABSTRACT EP 817068 A1
An apparatus for facilitating the sharing of memory blocks between a computer node and an external device irrespective whether the external device and the common bus both employ a common protocol and irrespective whether the external device and the common bus both operate at the same speed. Each of the memory blocks has a local physical address at a memory module of the computer node and an associated Mtag for tracking a state associated with that memory block, including a state for indicating whether that memory block is exclusive to the computer node, a state for indicating whether that memory block is shared by the computer node with the external device, and a state for indicating whether that memory block is invalid in the computer node. The apparatus includes receiver logic configured for coupling with a common bus of the computer node, the receiver logic being configured to receive, when coupled to the common bus, memory access requests specific to the apparatus on the common bus. There is further included a protocol transformer logic coupled to the receiver logic for enabling the apparatus, when coupled to the external device, to communicate with the external device using a protocol suitable for communicating with the external device.
ABSTRACT WORD COUNT: 206

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	010110 A1	Date of dispatch of the first examination report: 20001123
Application:	980107 A1	Published application (A1with Search Report ;A2without Search Report)
Assignee:	030423 A1	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Examination:	980729 A1	Date of filing of request for examination: 980527
Change:	980916 A1	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9802	3015
SPEC A	(English)	9802	9063
Total word count - document A			12078
Total word count - document B			0
Total word count - documents A + B			12078

4/5/16 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00893681
Methods and apparatus for a coherence transformer for connecting computer system coherence domains
Verfahren und Vorrichtung fur einen Koharenzumwandler zur Verbindung von Rechnersystemkoharenzdomanen
Procede et dispositif pour transformateur de coherence permettant la connexion des domaines de coherence de systeme d'ordinateur
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)

INVENTOR:
Hagerstein,Erik E, 3451 Cork Oak Way, Palo Alto CA 94043, (US)
Hill , Mark Donald , 2124 Chamberlain Avenue, Madison WI 53705, (US)
Wood , David A. , 2115 Bascom Street, Madison WI 53705, (US
LEGAL REPRESENTATIVE:
Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 817065 A1 980107 (Basic)
EP 817065 B1 030917
APPLICATION (CC, No, Date): EP 97304519 970625;
PRIORITY (CC, No, Date): US 677015 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**
CITED PATENTS (EP B): EP 392657 A; EP 801349 A
CITED REFERENCES (EP B):
LENOSKI D ET AL: "THE STANFORD DASH MULTIPROCESSOR" COMPUTER, vol. 25, no. 3, March 1992, pages 63-79, XP000288291
O'KRAFKA B W ET AL: "AN EMPIRICAL EVALUATION OF TWO MEMORY-EFFICIENT DIRECTORY METHODS" PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, SEATTLE, MAY 28 - 31, 1990, no. SYMP. 17, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 138-147, XP000144792
LOVETT T ET AL: "STING: A CC-NUMA COMPUTER SYSTEM FOR THE COMMERCIAL MARKETPLACE" COMPUTER ARCHITECTURE NEWS, vol. 24, no. 2, May 1996, pages 308-317, XP000592195;

ABSTRACT EP 817065 A1
An apparatus for facilitating the sharing of memory blocks, which has local physical addresses at a computer node, between the computer node and an external device. The apparatus includes snooping logic configured for coupling with a common bus of the computer node. The snooping logic is configured to monitor, when coupled to the common bus, memory access requests on the common bus. There is also included a snoop tag array coupled to the snooping logic. The snoop tag array includes tags for tracking all copies of a first plurality of memory blocks of the memory blocks cached by the external device. Further, there is included a protocol transformer logic coupled to the snooping logic for enabling the apparatus, when coupled to the external device, to communicate with the external device using a protocol suitable for communicating with the external device.
ABSTRACT WORD COUNT: 141
NOTE:
Figure number on first page: 3

LEGAL STATUS (Type, Pub Date, Kind, Text):
Examination: 010103 A1 Date of dispatch of the first examination report: 20001115
Application: 980107 A1 Published application (A1with Search Report ;A2without Search Report)
Grant: 030917 B1 Granted patent
Assignee: 030423 A1 Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Examination: 980708 A1 Date of filing of request for examination: 980508
Change: 980916 A1 Designated Contracting States (change)
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199802	2332
CLAIMS B	(English)	200338	1639
CLAIMS B	(German)	200338	1557
CLAIMS B	(French)	200338	1801
SPEC A	(English)	199802	9615
SPEC B	(English)	200338	9923

Total word count - document A 11949
Total word count - document B 14920

Total word count - documents A + B 26869

4/5/17 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00893677
Methods and apparatus for a directory less memory access protocol in a distributed shared memory computer system
Verfahren und Vorrichtung fur ein verzeichnisloses Speicherzugriffsprotokoll in einem Rechnersystem mit verteiltem gemeinsamen Speicher
Procedes et dispositif pour un protocole d'acces a memoire sans repertoire dans un systeme d'ordinateur avec memoire partagee repartie

PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, CA 94043, (US)
Hill, Mark Donald , 2124 Chamberlain Avenue, Madison, WI 53705, (US
LEGAL REPRESENTATIVE:
Turner, James Arthur et al (74631), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 817064 A2 980107 (Basic)
EP 817064 A3 980204
EP 817064 B1 030507
APPLICATION (CC, No, Date): EP 97304515 970625;
PRIORITY (CC, No, Date): US 671303 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**
CITED REFERENCES (EP B):
KUMAR A ET AL: "Efficient and scalable cache coherence schemes for shared memory hypercube multiprocessors" PROCEEDINGS SUPERCOMPUTING '94 (CAT. NO.94CH34819), PROCEEDINGS OF SUPERCOMPUTING '94, WASHINGTON, DC, USA, 14-18 NOV. 1994, ISBN 0-8186-6605-6, 1994, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC. PRESS, USA, pages 498-507, XP000533913
FARKAS K ET AL: "SCALABLE CACHE CONSISTENCY FOR HIERARCHICALLY STRUCTURED MULTIPROCESSORS" JOURNAL OF SUPERCOMPUTING, vol. 8, no. 4, 1 January 1995, pages 345-369, XP000589464
ARCHIBALD ET AL: "An economical solution to the cache coherence problem" THE 11TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, 5 - 7 June 1984, MICHIGAN; US, pages 355-361, XP002049370
GRAHN H ET AL: "EFFICIENT STRATEGIES FOR SOFTWARE-ONLY DIRECTORY PROTOCOLS IN SHARED-MEMORY MULTIPROCESSORS" COMPUTER ARCHITECTURE NEWS, vol. 23, no. 2, 1 May 1995, pages 38-47, XP000525159;

ABSTRACT EP 817064 A3
A method in a computer network having a first plurality of nodes coupled to a common network infrastructure and a distributed shared memory distributed among the first plurality of nodes for servicing a first memory access request by a first node of the computer network pertaining to a memory block having a home node different from the first node in the computer network. The computer network has no natural ordering mechanism and natural broadcast for servicing memory access requests from the plurality of nodes. The home node has no centralized directory for tracking states of the memory block in the plurality of nodes. The method includes the step of receiving via the common network infrastructure at the home node from the first node the first memory access request for the memory block. There is also included the step of sending, if the home node does not have a firt valid copy of the memorv block, a request from the home node to second plurality of nodes in the computer network to request a second node in the computer network to send the first valid copy of the memory block to the first node. The second plurality of nodes represents the first plurality of nodes excepting the first node and the home node. The first valid copy of the memory block represents a valid copy that is capable of servicing the first memory access request.

ABSTRACT WORD COUNT: 235
NOTE:
Figure number on first page: 6

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	000913 A2	Date of dispatch of the first examination report: 20000802
Application:	980107 A2	Published application (A1with Search Report ;A2without Search Report)
Lapse:	040107 B1	Date of lapse of European Patent in a contracting state (Country, date): NL 20030507, SE 20030807,
Grant:	030507 B1	Granted patent
Assignee:	030423 A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Lapse:	031210 B1	Date of lapse of European Patent in a contracting state (Country, date): SE 20030807,
Search Report:	980204 A3	Separate publication of the European or International search report
Examination:	980819 A2	Date of filing of request for examination: 980619
Change:	981014 A2	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199802	1918
CLAIMS B	(English)	200319	1327
CLAIMS B	(German)	200319	1293
CLAIMS B	(French)	200319	1458
SPEC A	(English)	199802	7712
SPEC B	(English)	200319	7435
Total word count - document A			9632
Total word count - document B			11513
Total word count - documents A + B			21145

4/5/18 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00844839
Hybrid numa coma caching system and methods for selecting between the caching modes
Hybrides NUMA/COMA-Cachespeicherungssystem und Verfahren zur Auswahl aus den Cachemoden
Systeme d'antememorisation de type NUMA/COMA hybride et procede de selection de mode d'antememorisation
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392730), 2550 Garcia Avenue, Mountain View, CA 94043, (US), (applicant designated states: GB;SE)
INVENTOR:
Wood, David , 2115 Bascom Street, Madison, Wisconsin 53705, (US)
Hagersten, Erik, 3451 Cork Oak Way, Palo Alto, California 94303, (US
LEGAL REPRESENTATIVE:
Harris, Ian Richard (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 780770 A1 970625 (Basic)
APPLICATION (CC, No, Date): EP 96309360 961220;
PRIORITY (CC, No, Date): US 575787 951222
DESIGNATED STATES: GB; SE
INTERNATIONAL PATENT CLASS: **G06F-012/08**

ABSTRACT EP 780770 A1
The present invention provides a hybrid Non-Uniform Memory Architecture (NUMA) and Cache-Only Memory Architecture (COMA) caching architecture

together with a cache-coherent protocol for a computer system having a plurality of sub-systems coupled to each other via a system interconnect. In one implementation, each sub-system includes at least one processor, a page-oriented COMA cache and a line-oriented hybrid NUMA/COMA cache. Such a hybrid system provides flexibility and efficiency in caching both large and small, and/or sparse and packed data structures. Each sub-system is able to independently store data in COMA mode or in NUMA mode. When caching in COMA mode, a sub-system allocates a page of memory space and then stores the data within the allocated page in its COMA cache. Depending on the implementation, while caching in COMA mode, the sub-system may also store the same data in its hybrid cache for faster access. Conversely, when caching in NUMA mode, the sub-system stores the data, typically a line of data, in its hybrid cache.

ABSTRACT WORD COUNT: 165

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	001213 A1	Date of dispatch of the first examination report: 20001027
Application:	970625 A1	Published application (A1with Search Report ;A2without Search Report)
Assignee:	030423 A1	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US
Change:	030108 A1	Legal representative(s) changed 20021121
Examination:	980304 A1	Date of filing of request for examination: 971222

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB97	1442
SPEC A	(English)	EPAB97	8242
Total word count - document A			9684
Total word count - document B			0
Total word count - documents A + B			9684

4/5/19 (Item 1 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

00480751 **Image available**

SCALABLE SHARED MEMORY MULTIPROCESSOR SYSTEM

SYSTEME MULTIPROCESSEUR A MEMOIRE COMMUNE POUVANT ETRE ECHELONNEE

Patent Applicant/Assignee:
SUN MICROSYSTEMS INC,

Inventor(s):
HAGERSTEN Erik E,
HILL Mark

Patent and Priority Information (Country, Number, Date):
Patent: WO 9912103 A2 19990311
Application: WO 98US18469 19980904 (PCT/WO US9818469)
Priority Application: US 97924385 19970905

Designated States: JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Main International Patent Class: **G06F-012/10**

International Patent Class: **G06F-012/08**

Publication Language: English

Fulltext Availability:
Detailed Description
Claims

Fulltext Word Count: 9120

English Abstract

A portion of the global memory of a multiprocessing computer system is allocated to each node, called local memory space. Data from a remote node may be copied to local memory space of a node such that accesses to the data may be performed locally rather than globally. The copied data is referred to as a shadow page. The global address of the data is translated to a local physical address for the node to which the data is

copied. To reduce the size of the translation tables for converting between global addresses and local physical addresses, the page to which shadow copies may be stored and which global addresses may be converted to local physical addresses may be restricted. Multiple page of local memory space may be allocated to one entry of a local physical address to global address (LPA2GA) table. When a page is allocated to store shadow pages, an entry in the LPA2GA table associated with that page is marked as unavailable. In a similar manner, multiple pages of the global address space are mapped to an entry in a global address to local physical address (GA2LPA) translation table. To decrease the probability that an entry is not available for a page, the GA2LPA table may be implemented as a set associative table. To further increase the availability of entries in the GA2LPA table, a skewed-associative cache that implements an insertion algorithm that realigns the translations in the table to maximize the utilization of the available entries is implemented. A coherent memory replication (CMR) address space stores shadow pages of data from remote nodes and a local address space stores local data. A bit within a local physical address identifies whether data is a shadow page, which is stored in CMR space, or local data, which is stored in local address space.

French Abstract

L'invention concerne un systeme informatique multiprocesseur dont une partie de la memoire globale est attribuee a chaque noeud, cette partie etant denommee espace memoire local. Des donnees provenant d'un noeud a distance peuvent etre copiees dans l'espace memoire local d'un noeud de sorte que l'acces aux donnees puisse s'effectuer de maniere locale plutot que globale. Les donnees copiees sont appelees pages d'ombre. L'adresse globale des donnees est traduite dans une adresse physique locale pour le noeud dans lequel les donnees sont copiees. Pour reduire la taille des tables de traduction destinees a la conversion entre les adresses globales et les adresses physiques locales, on peut reduire la page dans laquelle des copies d'ombre peuvent etre memorisees et dont les adresses globales peuvent etre converties en adresses physiques locales. Plusieurs pages d'un espace memoire local peuvent etre attribuees a une entree d'une table de conversion d'adresse physique locale en adresse globale (LPA2GA). Lorsqu'on attribue a une table la memorisation de pages d'ombre, une entree dans la table LPA2GA associee a cette page est indiquee comme non disponible. De la meme maniere, on fait correspondre plusieurs pages de l'espace d'adresse globale avec une entree dans une table de traduction d'adresse globale en adresse physique locale (GA2LPA). Pour reduire la probabilite qu'une entree ne soit pas disponible pour une page, on peut installer la table GA2LPA comme une table associative determinee. Pour augmenter d'avantage la disponibilite d'entrees dans la table GA2LPA, on installe une cache a associativite oblique executant un algorithme d'insertion qui aligne de nouveau les traductions dans la table pour maximiser l'utilisation des entrees disponibles. Un espace d'adresse de replication de memoire coherente (CMR) memorise des pages d'ombre de donnees provenant de noeuds a distance et un espace d'adresse locale memorise les donnees locales. Un element binaire se trouvant dans une adresse physique locale determine si les donnees sont une page d'ombre, memorisee dans un espace CMR, ou des donnees locales, memorisees dans un espace d'adresse locale.

4/5/20 (Item 1 from file: 350)

015833907 **Image available**

WPI Acc No: 2003-896111/200382
XRPX Acc No: N03-715040

Access providing shared memory for computer system, has controller to implement one set of rules in coherent mode of operation and another set of rules to provide copy of data in memory in read current mode of operation

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)

Inventor: COWAN J P; EBNER S M; **JACKSON C H** ; SHARMA D D; WICKERAAD J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6647469	B1	20031111	US 2000562191	A	20000501	200382	B

Priority Applications (No Type Date): US 2000562191 A 20000501
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6647469	B1		27	G06F-012/00	

Abstract (Basic): US 6647469 B1

NOVELTY - The memory has a controller (130) that provides memory access to the agents in both coherent and read current modes of operation. The controller implements a set of rules in the coherent mode of operation to insure that all copies of data stored by the agents are coherent with the data stored in the memory. Another set of rules is implemented to provide a copy of the data stored in the memory in the read current mode.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of providing memory access to agents.

USE - Used for providing access to a shared memory in a computer system.

ADVANTAGE - The set of rules in the read current mode of operation copies the data to the agent, thereby eliminating the possibility of data from becoming stale and misused by another agent. The data obtained is limited in a boundary that restricts the read current data from causing data corruption. The set of rules improve the useable bandwidth for large payload transfers within few steps.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram with a shared memory.

Cell (105)
System interconnect (115)
Processor bus (120)
System memory controller (130)
Main memory (135)
pp; 27 DwgNo 1/20

Title Terms: ACCESS; SHARE; MEMORY; COMPUTER; SYSTEM; CONTROL; IMPLEMENT; ONE; SET; RULE; COHERE; MODE; OPERATE; SET; RULE; COPY; DATA; MEMORY; READ; CURRENT; MODE; OPERATE
Derwent Class: T01
International Patent Class (Main): **G06F-012/00**
File Segment: EPI

4/5/23 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015504527 **Image available**
WPI Acc No: 2003-566674/200353
XRPX Acc No: N03-450476

Cache structure for computer, determines fetch size value using sub-block use table which includes entries indicating sub-blocks loaded by miss processing circuit

Patent Assignee: WISCONSIN ALUMNI RES FOUND (WISC)
Inventor: BURGER D C; **WOOD D A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6557080	B1	20030429	US 99117148	P	19990125	200353	B
			US 2000490842	A	20000125		

Priority Applications (No Type Date): US 99117148 P 19990125; US 2000490842 A 20000125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

US 6557080 B1 10 G06F-012/08 Provisional application US 99117148

Abstract (Basic): US 6557080 B1

NOVELTY - A miss processing circuit responds to request from a processor (12) for data of a given sub-block (24) not in a cache (16), by loading requested data into several sub-blocks which are not requested by the processor as determined by fetch size value (38). A sub-block use table (32) to determine fetch size value, has entries indicating sub-blocks loaded by the miss processing circuit and which are provided with data after loading.

USE - Cache structure for computer.

ADVANTAGE - Appropriate fetch block size is determined to satisfy the requirement of minimized cache misses and minimized superfluous traffic between memory and cache.

DESCRIPTION OF DRAWING(S) - The figure shows the cache structure with a sub-block use table.

processor (12)
cache (16)
sub-block (24)
sub-block use table (32)
fetch size value (38)
pp; 10 DwgNo 2/7

Title Terms: CACHE; STRUCTURE; COMPUTER; DETERMINE; FETCH; SIZE; VALUE; SUB ; BLOCK; TABLE; ENTER; INDICATE; SUB; BLOCK; LOAD; MISS; PROCESS; CIRCUIT
Derwent Class: T01
International Patent Class (Main): **G06F-012/08**
File Segment: EPI

4/5/24 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015430491 **Image available**
WPI Acc No: 2003-492633/200346
XRPX Acc No: N03-391327

Virtual memory control method in computer system, involves setting translation entry mapping indicator for each entry associated with given context of memory and demapping given context by changing set mapping indicator

Patent Assignee: CASSIDAY D R (CASS-I); FEEHRER J R (FEEH-I); HILL M D (HILL-I); JACKSON C J (JACK-I); OSTROVSKY B (OSTR-I); PILLAI P (PILL-I); WOOD D A (WOOD-I)
Inventor: **CASSIDAY D R ; FEEHRER J R ; HILL M D ; JACKSON C J ; OSTROVSKY B ; PILLAI P ; WOOD D A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030070058	A1	20030410	US 2001973279	A	20011009	200346	B

Priority Applications (No Type Date): US 2001973279 A 20011009
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030070058	A1		10	G06F-012/10	

Abstract (Basic): US 20030070058 A1

NOVELTY - A translation entry mapping indicator (132) is set for each entry associated with the given context (134) of memory and a validity flag (130) is set for each entry associated with the given context. The given context is demapped by changing the mapping indicator set for each given context.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory management device; and program for controlling virtual memory in computer system.

USE - For controlling physical memory of computer system.

ADVANTAGE - The time required to demap the given context is reduced without degrading the performance of the computer system. Thereby the

memory management process is performed efficiently.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of memory management unit.
context mapping indicator (122)
clean-up indicator (124)
validity flag (130)
translation entry mapping indicator (132)
context (134)
pp; 10 DwgNo 2/5

Title Terms: VIRTUAL; MEMORY; CONTROL; METHOD; COMPUTER; SYSTEM; SET; TRANSLATION; ENTER; MAP; INDICATE; ENTER; ASSOCIATE; CONTEXT; MEMORY; CONTEXT; CHANGE; SET; MAP; INDICATE
Derwent Class: T01
International Patent Class (Main): **G06F-012/10**
File Segment: EPI

4/5/26 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014735491 **Image available**
WPI Acc No: 2002-556195/200259
Related WPI Acc No: 1999-214777; 1999-229005; 2001-440315; 2001-625048; 2001-662307; 2002-113100; 2002-130078; 2002-216172; 2002-360426; 2002-498165; 2003-606485
XRPX Acc No: N02-440157

Multiprocessing computer system has request agent of system interface coupled to error status registers that store error information of transactions initiated by processors

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: GUZOVSKIY A; HAGERSTEN E E; **JACKSON C J** ; NESHEIM W A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6401174	B1	20020604	US 97924385	A	19970905	200259	B
			US 98148734	A	19980904		

Priority Applications (No Type Date): US 98148734 A 19980904; US 97924385 A 19970905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6401174	B1		28	G06F-012/00	CIP of application US 97924385

Abstract (Basic): US 6401174 B1
NOVELTY - A system interface has error status registers to store error information of transactions initiated by processors through a local bus. The system interface includes a request agent coupled to the error status registers.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for error information communicating method in multiprocessing system.
USE - Multiprocessing computer system.
ADVANTAGE - Supports disclosed error reporting mechanism that provides virtualized error information without processor faults or traps.
DESCRIPTION OF DRAWING(S) - The figure shows the flowchart for error reporting in multiprocessor computer system.
pp; 28 DwgNo 7/11

Title Terms: MULTIPROCESSOR; COMPUTER; SYSTEM; REQUEST; AGENT; SYSTEM; INTERFACE; COUPLE; ERROR; STATUS; REGISTER; STORAGE; ERROR; INFORMATION; TRANSACTION; INITIATE; PROCESSOR
Derwent Class: T01
International Patent Class (Main): **G06F-012/00**
File Segment: EPI

4/5/27 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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014687874 **Image available**
WPI Acc No: 2002-508578/200254
Related WPI Acc No: 2002-508139; 2002-508140; 2002-508149; 2002-558129; 2002-698688
XRPX Acc No: N02-402472

Remote small computer system interface device identification method in Internet protocol data network, involves notifying data about existence of SCSI device to network management system

Patent Assignee: PIRUS NETWORKS (PIRU-N); GROSNER G (GROS-I); WOOD D (WOOD-I)
Inventor: GROSNER G; **WOOD D**
Number of Countries: 096 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200246866	A2	20020613	WO 2001US45771	A	20011102	200254 B
AU 200241559	A	20020618	AU 200241559	A	20011102	200262
US 20040044744	A1	20040304	WO 2001US45771	A	20011102	200417
			US 2003415314	A	20030903	

Priority Applications (No Type Date): US 2000245295 P 20001102; US 2003415314 A 20030903
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200246866	A2	E	166	G06F-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200241559	A	G06F-000/00	Based on patent WO 200246866
US 20040044744	A1	G06F-015/16	

Abstract (Basic): WO 200246866 A2

NOVELTY - A request to identify a remote small computer system interface (SCSI) device is received at a switch element. An address resolution protocol (ARP) entry for the SCSI device is returned based on the request. A SCSI read request is transmitted from the switch element to the SCSI device and data about existence of SCSI device is notified to network management system.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Method of enabling the NMS to receive SNMP traps in response to generation of SCSI exceptions by the remote SCSI device; and

(2) IP data network.

USE - For identifying remote SCSI device IP data network (claimed).

ADVANTAGE - Enables automatic identification of SCSI devices over the IP network and mapping of SNMP requests to SCSI. Provides WAN mediation caching on local devices.

DESCRIPTION OF DRAWING(S) - The figure shows the architecture of the switch system.

pp; 166 DwgNo 1/46

Title Terms: REMOTE; COMPUTER; SYSTEM; INTERFACE; DEVICE; IDENTIFY; METHOD; PROTOCOL; DATA; NETWORK; NOTIFICATION; DATA; EXIST; DEVICE; NETWORK; MANAGEMENT; SYSTEM
Derwent Class: T01; W01
International Patent Class (Main): **G06F-000/00 ; G06F-015/16**
International Patent Class (Additional): **G06F-012/00**
File Segment: EPI

4/5/28 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

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014604542 **Image available**
WPI Acc No: 2002-425246/200245
XRPX Acc No: N02-334380

Locked transaction permitting method within computer system, involves changing status of register to quiesce system, when shared resource required for transaction is obtained

Patent Assignee: BLAKELY R J (BLAK-I); FEEHRER J R (FEEH-I); MORRISON J A (MORR-I); RENTSCHLER E M (RENT-I); HEWLETT-PACKARD CO (HEWP)
Inventor: BLAKELY R J; **FEEHRER J R** ; MORRISON J A; RENTSCHLER E M
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020038398	A1	20020328	US 99277718	A	19990326	200245	B
US 6381663	B1	20020430	US 99277718	A	19990326	200245	

Priority Applications (No Type Date): US 99277718 A 19990326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020038398	A1		10	G06F-013/00	
US 6381663	B1			G06F-013/00	

Abstract (Basic): US 20020038398 A1

NOVELTY - A request for locked transaction is detected through a 32-bit bus (116). The status of a register is changed to quiesce the computer system, when a shared resource required for transaction is obtained. The locked transaction is sent through a 64-bit bus (115) for execution.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for locked transaction permitting apparatus.

USE - For permitting locked transaction within computer system.

ADVANTAGE - The controllers function effectively to permit bus locking in a system having a bus that does not use traditional bus locking.

DESCRIPTION OF DRAWING(S) - The figure shows the computer system.

64-bit bus (115)
32-bit bus (116)
pp; 10 DwgNo 1/3

Title Terms: LOCK; TRANSACTION; PERMIT; METHOD; COMPUTER; SYSTEM; CHANGE; STATUS; REGISTER; SYSTEM; SHARE; RESOURCE; REQUIRE; TRANSACTION; OBTAIN
Derwent Class: T01; U21
International Patent Class (Main): **G06F-013/00**
International Patent Class (Additional): **G06F-012/00** ; **G06F-012/14**
File Segment: EPI

4/5/29 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014395469 **Image available**
WPI Acc No: 2002-216172/200227
Related WPI Acc No: 1999-214777; 1999-229005; 2001-440315; 2001-625048; 2001-662307; 2002-113100; 2002-130078; 2002-360426; 2002-498165; 2002-556195; 2003-606485
XRPX Acc No: N02-165668

Look-up table in multiprocessor computer system, has address circuit which determines alternate address if both primary and secondary entries are not available

Patent Assignee: HAGERSTEN E E (HAGE-I); HILL M D (HILL-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020019921	A1	20020214	US 97924385	A	19970905	200227	B
			US 98148820	A	19980904		

			US 2001940172	A	20010827	
US 6654866	B2	20031125	US 97924385	A	19970905	200378
			US 98148820	A	19980904	
			US 2001940172	A	20010827	

Priority Applications (No Type Date): US 98148820 A 19980904; US 97924385 A 19970905; US 2001940172 A 20010827

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020019921	A1		37	G06F-012/00	CIP of application US 97924385 Cont of application US 98148820 Cont of patent US 6308246
US 6654866	B2			G06F-012/10	CIP of application US 97924385 Cont of application US 98148820 Cont of patent US 6308246

Abstract (Basic): US 20020019921 A1

NOVELTY - An address circuit converts input address to primary and secondary look-up addresses which correspond to primary and secondary entries. A data corresponding to the input address, is stored in the primary entry if primary entry is available, otherwise data is stored in the secondary entry. If both primary and secondary entries are not available, an alternate address is determined.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Data storage and retrieval method;

(b) Method of increasing utilization of look-up table

USE - For storing data corresponding to input address in multiprocessor computer systems.

ADVANTAGE - The access time of the look-up table is minimized and utilization of the table is maximized by realigning data stored in the table if an entry for new data is not available.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the multiprocessor computer system.

pp; 37 DwgNo 1/14

Title Terms: UP; TABLE; MULTIPROCESSOR; COMPUTER; SYSTEM; ADDRESS; CIRCUIT; DETERMINE; ALTERNATE; ADDRESS; PRIMARY; SECONDARY; ENTER; AVAILABLE

Derwent Class: T01

International Patent Class (Main): **G06F-012/00 ; G06F-012/10**

International Patent Class (Additional): **G06F-012/12**

File Segment: EPI

4/5/30 (Item 11 from file: 350)

014309375 **Image available**

WPI Acc No: 2002-130078/200217

Related WPI Acc No: 1999-214777; 1999-229005; 2001-440315; 2001-625048; 2001-662307; 2002-113100; 2002-216172; 2002-360426; 2002-498165; 2002-556195; 2003-606485

XRPX Acc No: N02-098123

Multiprocessing computer system e.g. SMP computer system selects particular entry of memory management unit for controlling operation of local bus, in response to global transaction received by system interface

Patent Assignee: GUZOVSKIY A (GUZO-I); HAGERSTEN E E (HAGE-I); JACKSON C J (JACK-I); NESHEIM W A (NESH-I); SUN MICROSYSTEMS INC (SUNM)

Inventor: GUZOVSKIY A; HAGERSTEN E E; **JACKSON C J** ; NESHEIM W A

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020004886	A1	20020110	US 97924385	A	19970905	200217	B
			US 98148735	A	19980904		
US 6449700	B2	20020910	US 97924385	A	19970905	200263	
			US 98148735	A	19980904		

Priority Applications (No Type Date): US 98148735 A 19980904; US 97924385 A 19970905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020004886	A1		29	G06F-012/08	CIP of application US 97924385
US 6449700	B2			G06F-012/00	CIP of application US 97924385

Abstract (Basic): US 20020004886 A1

NOVELTY - A system interface (24) coupled between a global bus and local bus, receives global transaction including address from the remote node (12). The address is used for selecting particular entry of memory management unit (76). The selected entry has a field including a specific value for controlling the operation of local bus, in response to global transaction.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method of operating a multiprocessing computer system.

USE - Multiprocessing computer system e.g. symmetric multiprocessing computer system.

ADVANTAGE - Enables a node to control the resources used by remote cluster nodes and simple cluster communication protocols are implemented at the global level. Access restrictions are specified flexibly without the requirement of large memory capacity.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of symmetric multiprocessing node depicted multiprocessor computer system.

Remote node (12)
System interface (24)
Memory management unit (76)
pp; 29 DwgNo 2/11

Title Terms: MULTIPROCESSOR; COMPUTER; SYSTEM; COMPUTER; SYSTEM; SELECT; ENTER; MEMORY; MANAGEMENT; UNIT; CONTROL; OPERATE; LOCAL; BUS; RESPOND; GLOBE; TRANSACTION; RECEIVE; SYSTEM; INTERFACE
Derwent Class: T01
International Patent Class (Main): **G06F-012/00 ; G06F-012/08**
File Segment: EPI

4/5/31 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014178079 **Image available**
WPI Acc No: 2001-662307/200176
Related WPI Acc No: 1999-214777; 1999-229005; 2001-440315; 2001-625048; 2002-113100; 2002-130078; 2002-216172; 2002-360426; 2002-498165; 2002-556195; 2003-606485
XRPX Acc No: N01-493390

Look-up table for multiprocessor computer system, moves specified datum from primary entry to alternate entry, if both primary and secondary entries are not available for new datum

Patent Assignee: HAGERSTEN E E (HAGE-I); HILL M (HILL-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M ; HILL M D**
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6308246	B1	20011023	US 97924385	A	19970905	200176	B
			US 98148820	A	19980904		
US 20010042176	A1	20011115	US 97924385	A	19970905	200176	
			US 98148820	A	19980904		

Priority Applications (No Type Date): US 98148820 A 19980904; US 97924385 A 19970905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6308246	B1		37	G06F-012/10	CIP of application US 97924385
US 20010042176	A1			G06F-012/08	CIP of application US 97924385

Abstract (Basic): US 6308246 B1

NOVELTY - A look-up address circuit receives input address and converts into primary or secondary look-up addresses relative to primary or secondary entry. Look-up table stores a datum in primary entry if primary entry is available, else stores in secondary entry and moves a specified datum from primary entry to alternate entry if both the entries are not available for the datum, to store the datum in primary entry.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for data storing and retrieving method.

USE - For multiprocessor computer system.

ADVANTAGE - Since the method provides an entry to store new datum by moving the datum in primary entries to alternative entry, table utilization is increased, thereby approaches utilization of fully associative table.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of symmetric multiprocessing node.

pp; 37 DwgNo 2/14

Title Terms: UP; TABLE; MULTIPROCESSOR; COMPUTER; SYSTEM; MOVE; SPECIFIED; DATA; PRIMARY; ENTER; ALTERNATE; ENTER; PRIMARY; SECONDARY; ENTER; AVAILABLE; NEW; DATA

Derwent Class: T01

International Patent Class (Main): **G06F-012/08 ; G06F-012/10**

International Patent Class (Additional): **G06F-012/12**

File Segment: EPI

4/5/32 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013592183 **Image available**

WPI Acc No: 2001-076390/200109

XRPX Acc No: N01-058271

Address error recovery procedure for computer, involves reading out corresponding coherent condition from cache and calling recovery route to rectify the error

Patent Assignee: HEWLETT-PACKARD CO (HEWP)

Inventor: **FEEHRER J R ;** GAITHER B D; MORRISON J A

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000322317	A	20001124	JP 2000110434	A	20000412	200109	B
US 6405322	B1	20020611	US 99290942	A	19990413	200244	

Priority Applications (No Type Date): US 99290942 A 19990413

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000322317	A		11	G06F-012/08	
US 6405322	B1			G06F-012/16	

Abstract (Basic): JP 2000322317 A

NOVELTY - The address error which occurs in local channel (130) of computer system (100) is detected. The corresponding coherency condition is read from one or more address line specified from cache memory (120) and recovery routine is called for rectifying the address error.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for address error recovery system.

USE - For recovering address error in computers and processors.

ADVANTAGE - The cache coherency information is utilized, hence address error is easily detected.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of multiprocessor computing system.

Computer system (100)

Cache memory (120)

Local channel (130)
pp; 11 DwgNo 5/5
Title Terms: ADDRESS; ERROR; RECOVER; PROCEDURE; COMPUTER; READ; CORRESPOND ; COHERE; CONDITION; CACHE; CALL; RECOVER; ROUTE; RECTIFY; ERROR
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-012/16**
International Patent Class (Additional): **G06F-015/16 ; G06F-015/177**
File Segment: EPI

4/5/33 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013429147 **Image available**
WPI Acc No: 2000-601090/200057
XRPX Acc No: N00-444714

Backup memory storage apparatus for digital data processing system has memory to store audit trail entries based on indication of controller which comprises request of audit trail entries

Patent Assignee: UNISYS CORP (BURS)
Inventor: COOPER T P; **HILL M J** ; KONRAD D R; NOWATZKI T L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6079000	A	20000620	US 971136	A	19971230	200057	B

Priority Applications (No Type Date): US 971136 A 19971230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6079000	A		27	G06F-012/00	

Abstract (Basic): US 6079000 A
NOVELTY - A controller is coupled to three memory units. A portion of audit trail entries from third memory is stored in first memory until an indication is received from the controller, where the indication comprises synchronous audit data request of audit trail entries having a commit in progress status.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for backup memory storage method.
USE - For digital data processing system.
ADVANTAGE - Since the memory stores audit trail entries based on indication of controller which comprises request of audit trail entries having commit in progress status, the transfer efficiency of audit trail entries is improved.
DESCRIPTION OF DRAWING(S) - The figure shows the flow chart explaining the backup memory storage method.
pp; 27 DwgNo 11A,11B/12
Title Terms: MEMORY; STORAGE; APPARATUS; DIGITAL; DATA; PROCESS; SYSTEM; MEMORY; STORAGE; AUDIT; TRAILING; ENTER; BASED; INDICATE; CONTROL; COMPRISE; REQUEST; AUDIT; TRAILING; ENTER
Derwent Class: T01
International Patent Class (Main): **G06F-012/00**
File Segment: EPI

4/5/34 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013064745 **Image available**
WPI Acc No: 2000-236617/200020
XRPX Acc No: N00-177379

System for organizing and managing recovery information on a per transaction basis using distinct memory structures

Patent Assignee: UNISYS CORP (BURS)
Inventor: COOPER T P; **HILL M J** ; KONRAD D R; NOWATZKI T L

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6018746	A	20000125	US 97996760	A	19971223	200020	B

Priority Applications (No Type Date): US 97996760 A 19971223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6018746	A		17	G06F-012/08	

Abstract (Basic): US 6018746 A

NOVELTY - The memory architecture comprises several storage modules for holding transaction recovery information and several memory structures corresponding to a distinct transaction to isolate accessibility of the recovery information. Each memory structure comprises a control information field and several information address fields. The memory structures are non-volatile RAM and are arranged in a linked list. Also included is an INDEPENDENT CLAIM for a transaction processing system.

USE - For use in a multi-processing environment such as airline or banking systems.

ADVANTAGE - Prevents loss of transaction information. Provides a centralized, commonly accessible system for effecting recovery actions in a data processing system.

DESCRIPTION OF DRAWING(S) - The figure is a block diagram of system providing task management.

pp; 17 DwgNo 2/8

Title Terms: SYSTEM; MANAGE; RECOVER; INFORMATION; PER; TRANSACTION; BASIS; DISTINCT; MEMORY; STRUCTURE
Derwent Class: T01
International Patent Class (Main): **G06F-012/08**
International Patent Class (Additional): **G06F-012/02**
File Segment: EPI

4/5/35 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012422897 **Image available**
WPI Acc No: 1999-229005/199919
Related WPI Acc No: 1999-214777; 2001-440315; 2001-625048; 2001-662307; 2002-113100; 2002-130078; 2002-216172; 2002-360426; 2002-498165; 2002-556195; 2003-606485
XRPX Acc No: N99-169448

Address translations for clusters of multiprocessor systems

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M**
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9912103	A2	19990311	WO 98US18469	A	19980904	199919	B
EP 1019840	A2	20000719	EP 98944751	A	19980904	200036	
			WO 98US18469	A	19980904		
JP 2001515244	W	20010918	WO 98US18469	A	19980904	200169	
			JP 2000509039	A	19980904		
EP 1019840	B1	20031119	EP 98944751	A	19980904	200377	
			WO 98US18469	A	19980904		
DE 69819927	E	20031224	DE 619927	A	19980904	200408	
			EP 98944751	A	19980904		
			WO 98US18469	A	19980904		

Priority Applications (No Type Date): US 97924385 A 19970905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9912103	A2	E	58	G06F-015/00	

Designated States (National): JP

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
EP 1019840 A2 E Based on patent WO 9912103
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 2001515244 W 118 G06F-015/177 Based on patent WO 9912103
EP 1019840 B1 E G06F-012/10 Based on patent WO 9912103
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
DE 69819927 E G06F-012/10 Based on patent EP 1019840
Based on patent WO 9912103

Abstract (Basic): WO 9912103 A2

NOVELTY - The multiprocessor system has symmetrical multiprocessor nodes connected with other nodes to form clusters. The nodes have interfaces (24) with input (84) and output (86) request queues. Tables (80,82) handle translations between global and local addresses. Memory areas can be set up as shadow pages. The global to local address translation table is set associative. An insertion algorithm is used in this skewed associative cache to realign translations for maximum utilization.

USE - Global address translation in cluster systems

ADVANTAGE - By using set associative and an insertion algorithm the access time and memory needed are optimized.

DESCRIPTION OF DRAWING(S) - Cluster node interface

System interface (24)

Network I/O queues (84,86)

Global/Local address translation tables (80,82)

Queues to symmetrical processor node (92,96)

Access control agents (100,504)

Cluster memory management (504)

pp; 58 DwgNo 3/14

Title Terms: ADDRESS; TRANSLATION; CLUSTER; MULTIPROCESSOR; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-012/10 ; G06F-015/00 ; G06F-015/177**
International Patent Class (Additional): A01N-001/00; **G06F-012/08 ; G06F-012/12 ; G06F-015/16**
File Segment: EPI

4/5/36 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012408669 **Image available**
WPI Acc No: 1999-214777/199918
Related WPI Acc No: 1999-229005; 2001-440315; 2001-625048; 2001-662307; 2002-113100; 2002-130078; 2002-216172; 2002-360426; 2002-498165; 2002-556195; 2003-606485
XRPX Acc No: N99-158086

Cluster optimization interface for multiprocessing system

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: GUZOVSKIY A; HAGERSTEN E; **JACKSON C J** ; NESHEIM W A; NGUYEN H
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9912102	A1	19990311	WO 98US18466	A	19980904	199918	B
EP 1010090	A1	20000621	EP 98946854	A	19980904	200033	
			WO 98US18466	A	19980904		
JP 2001515243	W	20010918	WO 98US18466	A	19980904	200169	
			JP 2000509038	A	19980904		
EP 1010090	B1	20030813	EP 98946854	A	19980904	200355	
			WO 98US18466	A	19980904		
DE 69817192	E	20030918	DE 617192	A	19980904	200369	
			EP 98946854	A	19980904		
			WO 98US18466	A	19980904		

Priority Applications (No Type Date): US 97924385 A 19970905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9912102	A1	E	54	G06F-012/14	
Designated States (National): JP					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1010090	A1	E		G06F-015/00	Based on patent WO 9912102
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 2001515243	W		103	G06F-015/16	Based on patent WO 9912102
EP 1010090	B1	E		G06F-015/00	Based on patent WO 9912102
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
DE 69817192	E			G06F-015/00	Based on patent EP 1010090 Based on patent WO 9912102

Abstract (Basic): WO 9912102 A1

NOVELTY - The multiprocessor system has symmetrical multiprocessor nodes connected with other nodes to form clusters. The nodes have interfaces (24) with input (84) and output (86) request queues. These are handled by cluster agents (100,502) that reference a cluster memory management unit (504) to determine valid accesses. The memory management unit includes values that dictate what type of operations are permitted on the local node by a remote node. Error status is also monitored.

USE - Access control for clustered processor nodes

ADVANTAGE - Provides communication protocols for interconnecting clusters under user and kernel level control.

DESCRIPTION OF DRAWING(S) - Cluster node interface

System interface (24)

Network I/O queues (84,86)

Queues to symmetrical processor node (92,96)

Access control agents (100,504)

Cluster memory management (504)

pp; 54 DwgNo 5/11

Title Terms: CLUSTER; OPTIMUM; INTERFACE; MULTIPROCESSOR; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-012/14 ; G06F-015/00 ; G06F-015/16**
International Patent Class (Additional): **G06F-009/312 ; G06F-012/10 ; G06F-015/167 ; G06F-015/177**
File Segment: EPI

4/5/37 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011648549 **Image available**
WPI Acc No: 1998-065457/199807
XRPX Acc No: N98-051467

Computer network efficient communication facilitating - sets directory cache entry to determine which node in computer network currently possesses first valid copy of memory block

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 818732	A2	19980114	EP 97304524	A	19970625	199807	B
JP 10177518	A	19980630	JP 97187267	A	19970630	199836	
US 5864671	A	19990126	US 96673957	A	19960701	199911	
US 6243742	B1	20010605	US 96673957	A	19960701	200133	
			US 99236680	A	19990125		
US 6496854	B1	20021217	US 96673957	A	19960701	200307	

US 99236680 A 19990125
US 2000511882 A 20000225

Priority Applications (No Type Date): US 96673957 A 19960701; US 99236680 A 19990125; US 2000511882 A 20000225
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 818732	A2	E	24	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10177518	A		23	G06F-012/06	
US 5864671	A			G06F-012/00	
US 6243742	B1			G06F-015/167	Cont of application US 96673957 Cont of patent US 5864671
US 6496854	B1			G06F-012/00	Cont of application US 96673957 Cont of application US 99236680 Cont of patent US 5864671 Cont of patent US 6243742

Abstract (Basic): EP 818732 A
The method involves receiving via a common network infrastructure at a home node from the first node a first memory access request for a memory block (708). If directory states representing states of copies of the memory block on the first number of nodes are cached in a directory cache (702) entry of the partial directory cache, the first memory (704) access request is serviced using a directory protocol. This is performed by consulting the directory cache entry to determine which node in the computer network currently possesses a first valid copy of the memory block.
The latter represents a valid copy of the memory block that is capable of servicing the first memory access request. If the directory states related to the memory block are not cached in the partial directory cache, the first memory access request is serviced using a directory-less protocol.
ADVANTAGE - Permits directory entries corresponding to memory blocks of network distributed shared memory to be accessed in servicing memory access requests.
Dwg.10/12
Title Terms: COMPUTER; NETWORK; EFFICIENCY; COMMUNICATE; FACILITATE; SET; DIRECTORY; CACHE; ENTER; DETERMINE; NODE; COMPUTER; NETWORK; CURRENT; POSSESS; FIRST; VALID; COPY; MEMORY; BLOCK
Derwent Class: T01
International Patent Class (Main): **G06F-012/00 ; G06F-012/06 ; G06F-012/08 ; G06F-015/167**
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

4/5/38 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638451 **Image available**
WPI Acc No: 1998-055359/199806
Related WPI Acc No: 1998-055356
XRPX Acc No: N98-043863
Multiprocessor computer system with extended symmetrical architecture - has repeater that generates incoming control signal for controlling when first processor element receives transactions from first incoming queue
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D** ; SINGHAL A
Number of Countries: 020 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 817095	A2	19980107	EP 97304797	A	19970630	199806	B
JP 10187631	A	19980721	JP 97211430	A	19970702	199839	

US 5796605 A 19980818 US 96675361 A 19960702 199840
US 5805839 A 19980908 US 96675362 A 19960702 199843

Priority Applications (No Type Date): US 96675363 A 19960702; US 96675361 A 19960702; US 96675362 A 19960702
Cited Patents: -SR.Pub
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 817095 A2 E 27 G06F-015/16
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 10187631 A 101 G06F-015/16
US 5796605 A G06F-012/08
US 5805839 A G06F-013/00

Abstract (Basic): EP 817095 A

The system includes a repeater (34a) that receives incoming and transmits outgoing transactions. A first bus (34) is coupled to the repeater by the bus. The first bus includes a first incoming queue and a first processor element. The latter receives the incoming transactions from the repeater and the first processor element receives the outgoing transaction from the first incoming queue. The repeater generates an incoming control signal for controlling when the first processor element receives transactions from the first incoming queue.

The first processor element receives each of the outgoing transactions from the first incoming queue at approximately the same time as each of the outgoing transactions are received by other devices in the multiprocessor computer system.

USE - As architectural connection within multiprocessor computer system.

ADVANTAGE - Maintains memory coherency between each node. Allows maximum bus bandwidth to be used

Dwg.3/10

Title Terms: MULTIPROCESSOR; COMPUTER; SYSTEM; EXTEND; SYMMETRICAL; ARCHITECTURE; REPEATER; GENERATE; INCOMING; CONTROL; SIGNAL; CONTROL; FIRST; PROCESSOR; ELEMENT; RECEIVE; TRANSACTION; FIRST; INCOMING; QUEUE
Index Terms/Additional Words: SPARC; PROCESSOR; PERIPHERAL; COMPONENT; INTERCONNECTION
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-013/00 ; G06F-015/16**
International Patent Class (Additional): **G06F-013/36 ; G06F-013/40 ; G06F-015/163**
File Segment: EPI

4/5/39 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638448 **Image available**
WPI Acc No: 1998-055356/199806
Related WPI Acc No: 1998-055359
XRPX Acc No: N98-043860

Node in multiprocessor computer system - has first repeater that is coupled to top level interface by upper level bus, and including incoming queue and by-pass path

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 006
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
EP 817092 A2 19980107 EP 97304571 A 19970626 199806 B
JP 10097513 A 19980414 JP 97190730 A 19970702 199825
US 5754877 A 19980519 US 96675363 A 19960702 199827
JP 10187631 A 19980721 JP 97211430 A 19970702 199839
EP 817092 B1 20030827 EP 97304571 A 19970626 200358

DE 69724355 E 20031002 DE 624355 A 19970626 200372
EP 97304571 A 19970626

Priority Applications (No Type Date): US 96675363 A 19960702; US 96675361 A 19960702; US 96675362 A 19960702
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 817092 A2 E 25 G06F-015/16
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 10097513 A 25 G06F-015/173
US 5754877 A G06F-015/163
JP 10187631 A 101 G06F-015/16
EP 817092 B1 E G06F-015/173
Designated States (Regional): DE FR GB IT NL SE
DE 69724355 E G06F-015/173 Based on patent EP 817092

Abstract (Basic): EP 817092 A

The node includes a top level interface that receives incoming transactions and transmits outgoing transactions. The latter originate in the node and the incoming transaction do not originate in the node. An upper level bus (22) is provided and a first repeater (34).The latter is coupled to the top level interface by the upper level bus. The first repeater includes an incoming queue and a bypass path. The first repeater receives the incoming transactions from the top level interface and transmits the incoming transactions via the bypass path to a lower level bus (32).

The first repeater receives the outgoing transaction via the incoming queue to a lower level bus. The top level interface receives the incoming transactions on an unidirectional point-to-point link with another node. The top level interface transmits the outgoing transactions on an unidirectional point-to-point link with the another node.

USE - As symmetrical multiprocessor architecture.

ADVANTAGE - Maintains memory coherency between each node without using coherency state tags

Dwg.3/10

Title Terms: NODE; MULTIPROCESSOR; COMPUTER; SYSTEM; FIRST; REPEATER; COUPLE; TOP; LEVEL; INTERFACE; UPPER; LEVEL; BUS; INCOMING; QUEUE; PASS; PATH
Derwent Class: T01
International Patent Class (Main): **G06F-015/16 ; G06F-015/163 ; G06F-015/173**
International Patent Class (Additional): **G06F-012/08 ; G06F-013/36 ; G06F-013/40**
File Segment: EPI

4/5/40 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638437 **Image available**
WPI Acc No: 1998-055345/199806
XRPX Acc No: N98-043849
Computer system memory storage cacheing modes selecting - identifying at least two cache lines from among number of cache lines of lower level cache as storing components of data
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 003
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
EP 817080 A2 19980107 EP 97304726 A 19970630 199806 B
US 5802563 A 19980901 US 96674029 A 19960701 199842
JP 10214224 A 19980811 JP 97186076 A 19970627 199842

Priority Applications (No Type Date): US 96674029 A 19960701
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817080	A2	E	15	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10214224	A		20	G06F-012/08	
US 5802563	A			G06F-012/00	

Abstract (Basic): EP 817080 A

The method involves incrementally storing cache-line-sized components of a page-sized block of data in at least two of the cache lines of the lower level cache. A trigger for reviewing cache space allocation is then detected. At least two cache lines are identified from among the number of cache lines of the lower level cache as storing the components of the data. If the number of the identified at least two cache lines exceeds a threshold, then allocating one of the number of pages of the higher level cache.

The components are stored in at least two corresponding cache lines of the allocated page of the higher level cache.

ADVANTAGE - Provides efficient mechanism to select data structures for caching which optimises allocation of higher level cache memory space in multi-level computer system to maximise usage of cache and minimise overall assess time to data.

Dwg.4/5

Title Terms: COMPUTER; SYSTEM; MEMORY; STORAGE; MODE; SELECT; IDENTIFY; TWO ; CACHE; LINE; NUMBER; CACHE; LINE; LOWER; LEVEL; CACHE; STORAGE; COMPONENT; DATA
Index Terms/Additional Words: CACHE; ONLY; MEMORY; ARCHITECTURE; NON-UNIFORM
Derwent Class: T01
International Patent Class (Main): **G06F-012/00 ; G06F-012/08**
File Segment: EPI

4/5/41 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638436 **Image available**
WPI Acc No: 1998-055344/199806
XRPX Acc No: N98-043848

Method for replacing data within computer system having skip-level cache hierarchy - updating stale copy of data in higher-level cache, thus ensuring that any copy of data remaining in that cache is consistent with updated copy of data in home location

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 817079	A2	19980107	EP 97304725	A	19970630	199806	B
JP 11003280	A	19990106	JP 97184599	A	19970626	199911	
US 5903907	A	19990511	US 96674560	A	19960701	199926	
EP 817079	B1	20030903	EP 97304725	A	19970630	200360	
DE 69724533	E	20031009	DE 624533	A	19970630	200374	
			EP 97304725	A	19970630		

Priority Applications (No Type Date): US 96674560 A 19960701
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817079	A2	E	15	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 11003280	A		23	G06F-012/08	

US 5903907 A G06F-012/08
EP 817079 B1 E G06F-012/08
Designated States (Regional): DE FR GB IT NL SE
DE 69724533 E G06F-012/08 Based on patent EP 817079

Abstract (Basic): EP 817079 A

The method involves determining that a dirty copy of the data of a lower-level cache needs to be replaced by writing back the dirty copy from the lower-level cache to the home location, by updating the stale copy of data in the home location. The stale copy of the data in the higher-level cache is then updated or invalidated, thus ensuring that any copy of the data remaining in the upper-level cache is consistent with the updated copy of data in the home location.

The method further entails requesting an exclusive copy of the data from the home location. The dirty copy is written back from the lower-level cache to the home location, by updating the stale copy of data in the home location.

USE - In computer system memories.

ADVANTAGE - Provides flexible scheme for designating memory write back protocols for multiple level of memories within computer system for data coherency.

Dwg.1a/4

Title Terms: METHOD; REPLACE; DATA; COMPUTER; SYSTEM; SKIP; LEVEL; CACHE; HIERARCHY; UPDATE; STALE; COPY; DATA; HIGH; LEVEL; CACHE; ENSURE; COPY; DATA; REMAINING; CACHE; CONSISTENT; UPDATE; COPY; DATA; HOME; LOCATE
Index Terms/Additional Words: CACHE; ONLY; MEMORY; ARCHITECTURE; NON-UNIFORM
Derwent Class: T01
International Patent Class (Main): **G06F-012/08**
International Patent Class (Additional): **G06F-015/163**
File Segment: EPI

4/5/42 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638435 **Image available**
WPI Acc No: 1998-055343/199806
XRPX Acc No: N98-043847

Data to be cached in computer system selecting - determining if cache miss is to be avoidable cache miss, then cacheing data in cache

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 817078	A2	19980107	EP 97304723	A	19970630	199806 B
JP 10214229	A	19980811	JP 97184600	A	19970626	199842
US 5893150	A	19990406	US 96675306	A	19960701	199921

Priority Applications (No Type Date): US 96675306 A 19960701
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817078	A2	E	10	G06F-012/08	
	Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE				
JP 10214229	A		14	G06F-012/08	
US 5893150	A			G06F-012/12	

Abstract (Basic): EP 817078 A

The method involves searching for the data in a cache, then detecting a cache miss when the data cannot be found in the cache. If the cache miss is detected, then it requires fetching the data from a main memory. If the cache miss is determined to be the avoidable cache miss, then caching the data in the cache. The avoidable cache miss is

an excess cache miss or a capacity miss of the data or a conflict miss of the data.

The method further entails writing back any older data displaced from the cache to the main memory as a result of caching the data, while a count of the avoidable cache miss(es) of the data and a count of cache hit(s) of the older data are maintained. The data is cached and the older data is written back only if the count of the avoidable cache miss(es) exceeds the count of the cache hit(s).

ADVANTAGE - Minimises data fetches caused by cache misses since likelihood of data being accessed again increases dramatically if it has been accessed at least twice.

Dwg.3/3

Title Terms: DATA; COMPUTER; SYSTEM; SELECT; DETERMINE; CACHE; MISS; CACHE; MISS; DATA; CACHE
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-012/12**
International Patent Class (Additional): **G06F-015/163**
File Segment: EPI

4/5/43 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638428 **Image available**
WPI Acc No: 1998-055336/199806
XRPX Acc No: N98-043840

Migratory data access pattern detection and handling system for multiprocessor computer system - has multiple symmetric multiprocessor nodes interconnected by point to point network including cache, SMP bus, memory and system interface

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 817071	A2	19980107	EP 97304615	A	19970627	199806	B
US 5734922	A	19980331	US 96674330	A	19960701	199820	
JP 10143483	A	19980529	JP 97208225	A	19970630	199832	
EP 817071	B1	20030917	EP 97304615	A	19970627	200369	
DE 69724880	E	20031023	DE 624880	A	19970627	200377	
			EP 97304615	A	19970627		

Priority Applications (No Type Date): US 96674330 A 19960701
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817071	A2	E	34	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
US 5734922	A		38	G06F-012/04	
JP 10143483	A		143	G06F-015/16	
EP 817071	B1	E		G06F-012/08	
Designated States (Regional): DE FR GB IT NL SE					
DE 69724880	E			G06F-012/08	Based on patent EP 817071

Abstract (Basic): EP 817071 A

The system includes a directory at each node which stores coherency information for the coherency units for which that node is the home node. In addition, the directory stores a data access state corresponding to each coherency unit which indicates the data access pattern observed for that coherency unit.

The data access state may indicate migratory or non migratory data access patterns. If the coherency unit has been observed to have a migratory data access pattern, read or write access rights are granted. Conversely, if the coherency unit has been observed to have non migratory data access patterns, then read access rights are granted.

ADVANTAGE - increases performance by more efficient handling of migratory data access patterns while still handling the non migratory data access patterns efficiently.

Dwg.1/21

Title Terms: MIGRATION; DATA; ACCESS; PATTERN; DETECT; HANDLE; SYSTEM; MULTIPROCESSOR; COMPUTER; SYSTEM; MULTIPLE; SYMMETRICAL; MULTIPROCESSOR; NODE; INTERCONNECT; POINT; POINT; NETWORK; CACHE; BUS; MEMORY; SYSTEM; INTERFACE

Derwent Class: T01

International Patent Class (Main): **G06F-012/04 ; G06F-012/08 ; G06F-015/16**

International Patent Class (Additional): **G06F-013/16**

File Segment: EPI

4/5/44 (Item 25 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011638426 **Image available**

WPI Acc No: 1998-055334/199806

XRPX Acc No: N98-043838

Memory sharing method among coherence domains of computer system - by using coherence transformer and snoop tag array and memory status tag approaches

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: HAGERSTEIN E E; **HILL M D ; WOOD D A ;** HAGERSTEN E E

Number of Countries: 020 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 817069	A1	19980107	EP 97304526	A	19970625	199806	B
JP 10187633	A	19980721	JP 97187287	A	19970630	199839	
US 5829034	A	19981027	US 96677014	A	19960701	199850	
EP 817069	B1	20030502	EP 97304526	A	19970625	200330	
DE 69721394	E	20030605	DE 621394	A	19970625	200345	
			EP 97304526	A	19970625		

Priority Applications (No Type Date): US 96677014 A 19960701

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817069	A1	E	40	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10187633	A		34	G06F-015/16	
US 5829034	A			G06F-013/00	
EP 817069	B1	E		G06F-012/08	
Designated States (Regional): DE FR GB IT NL SE					
DE 69721394	E			G06F-012/08	Based on patent EP 817069

Abstract (Basic): EP 817069 A

The method involves using a coherence transformer to allow a computer node of one or more external devices to share memory blocks having local physical addresses at a memory module of the computer node. The coherence transformer includes logic for ascertaining whether a memory access request from the external device for a memory block should be responded to using a snoop only approach or a memory status tag only approach.

The snoop only approach requires a tag in a snoop tag array of the coherence transformer to be available to track the memory block for an entire duration that the memory block is cached by the external device. The memory status tag approach only temporarily stores the memory block until a global state associated with the memory block can be written back into the memory module of the computer node.

ADVANTAGE - Permits memory blocks having local physical address in particular computer node to be shared, in an efficient and error free manner, among interconnected entities such as internal processing nodes and external devices.

Dwg.7/15
Title Terms: MEMORY; SHARE; METHOD; COHERE; DOMAIN; COMPUTER; SYSTEM; COHERE; TRANSFORMER; TAG; ARRAY; MEMORY; STATUS; TAG; APPROACH
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-013/00 ; G06F-015/16**
International Patent Class (Additional): **G06F-012/06**
File Segment: EPI

4/5/45 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011638425 **Image available**
WPI Acc No: 1998-055333/199806
XRPX Acc No: N98-043837

Memory block sharing method between computer node and external device - by using memory state tag indicating in which of computer node and external mode data is valid also coherence transformer for protocol switching

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D ; WOOD D A**
Number of Countries: 020 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 817068	A1	19980107	EP 97304525	A	19970625	199806 B
JP 11003277	A	19990106	JP 97187268	A	19970630	199911
US 5940860	A	19990817	US 96677012	A	19960701	199939

Priority Applications (No Type Date): US 96677012 A 19960701
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817068	A1	E	26	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 11003277	A		32	G06F-012/06	
US 5940860	A			G06F-013/36	

Abstract (Basic): EP 817068 A

The method involves enabling sharing of memory blocks between a computer node and an external device irrespective of whether the external device and the common bus both employ a common protocol or both operate at the same speed. The method also involves employing apparatus in which each of the memory blocks has a local physical address at a memory module of the computer node and an associated memory state tag.

The state tag has states for indicating whether that memory block is exclusive to the computer node, is shared by the computer node with the external device or is invalid in the computer node. The apparatus includes receiver logic configured for coupling with a common bus of the computer node and to receive memory access requests specific to the apparatus on the common bus.

ADVANTAGE - Facilitates sharing irrespective of whether external device and common bus both employ common protocol and whether they operate at same speed.

Dwg.2/11
Title Terms: MEMORY; BLOCK; SHARE; METHOD; COMPUTER; NODE; EXTERNAL; DEVICE ; MEMORY; STATE; TAG; INDICATE; COMPUTER; NODE; EXTERNAL; MODE; DATA; VALID; COHERE; TRANSFORMER; PROTOCOL; SWITCH
Derwent Class: T01
International Patent Class (Main): **G06F-012/06 ; G06F-012/08 ; G06F-013/36**
International Patent Class (Additional): **G06F-013/42**
File Segment: EPI

4/5/46 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011638422 **Image available**
WPI Acc No: 1998-055330/199806
XRPX Acc No: N98-043834

Method of sharing memory among coherence domains of computer system - by using snoop tag array to track state of first copy of first memory block at external device

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEIN E E; **HILL M D** ; **WOOD D A** ; HAGERSTEN E E
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 817065	A1	19980107	EP 97304519	A	19970625	199806	B
JP 10214222	A	19980811	JP 97187281	A	19970630	199842	
US 5860109	A	19990112	US 96677015	A	19960701	199910	
EP 817065	B1	20030917	EP 97304519	A	19970625	200369	
DE 69724879	E	20031023	DE 624879	A	19970625	200377	
			EP 97304519	A	19970625		

Priority Applications (No Type Date): US 96677015 A 19960701
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817065	A1	E	24	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10214222	A		26	G06F-012/06	
US 5860109	A			G06F-012/00	
EP 817065	B1	E		G06F-012/08	
Designated States (Regional): DE FR GB IT NL SE					
DE 69724879	E			G06F-012/08	Based on patent EP 817065

Abstract (Basic): EP 817065 A

The method involves coupling to a common bus to obtain a first copy of a first memory block having a local physical address in the memory on behalf of an external device. A transformer receives the first memory access request for the first memory block from the external device, acquires the first copy of the first memory block from the common bus and uses a snoop tag array to track the state (exclusive, shared, invalid) of the first copy at the external device. the first copy is then sent to the external device from the transformer.

ADVANTAGE - Enables an external device to share memory blocks having local physical addresses in a memory module at the computer node, irrespective of whether the external device and common bus both employ a common protocol or whether they operate at the same speed.

Dwg.3/8

Title Terms: METHOD; SHARE; MEMORY; COHERE; DOMAIN; COMPUTER; SYSTEM; TAG; ARRAY; TRACK; STATE; FIRST; COPY; FIRST; MEMORY; BLOCK; EXTERNAL; DEVICE
Derwent Class: T01
International Patent Class (Main): **G06F-012/00** ; **G06F-012/06** ; **G06F-012/08**
File Segment: EPI

4/5/47 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011638421 **Image available**
WPI Acc No: 1998-055329/199806
XRPX Acc No: N98-043833

Directory less memory access protocol method for distributed shared memory computer system - By transferring requests between nodes for valid copy of memory block capable of servicing access request

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 817064	A2	19980107	EP 97304515	A	19970625	199806 B
JP 10134009	A	19980522	JP 97188917	A	19970701	199831
US 5873117	A	19990216	US 96671303	A	19960701	199914
US 6377980	B1	20020423	US 96671303	A	19960701	200232
			US 99236679	A	19990125	
EP 817064	B1	20030507	EP 97304515	A	19970625	200333
US 6574659	B1	20030603	US 96671303	A	19960701	200339
			US 99236679	A	19990125	
			US 2000531038	A	20000320	
DE 69721641	E	20030612	DE 621641	A	19970625	200346
			EP 97304515	A	19970625	

Priority Applications (No Type Date): US 96671303 A 19960701; US 99236679 A 19990125; US 2000531038 A 20000320
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817064	A2	E	17	G06F-012/08	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10134009	A		15	G06F-015/16	
US 5873117	A			G06F-013/14	
US 6377980	B1			G06F-015/167	Cont of application US 96671303 Cont of patent US 5873117
EP 817064	B1	E		G06F-012/08	
Designated States (Regional): DE FR GB IT NL SE					
US 6574659	B1			G06F-015/167	Cont of application US 96671303 Cont of application US 99236679 Cont of patent US 5873117 Cont of patent US 6377980
DE 69721641	E			G06F-012/08	Based on patent EP 817064

Abstract (Basic): EP 817064 A

The method involves using a computer network having multiple nodes connected to a common network infrastructure, and a shared memory distributed among the nodes, with no natural ordering mechanism and natural broadcast for servicing memory access requests from the nodes. The first node of the network is enabled to access a copy of a memory block having a home node which differs from the first, the home node having no centralised directory for storing memory block states in the nodes. The memory access request is received at the home node from the first node via the common network infrastructure, and the memory block status is marked as pending, rendering the home node incapable of servicing other memory access requests. If the home node has no valid copy of the memory block the home node requests the second set of nodes to send a second valid copy of the memory block to the first node. When this access request fulfilment acknowledgment is received the memory block status is marked as non-pend ing, allowing other memory access requests to be serviced.

ADVANTAGE - facilitates efficient communication in a computer network using distributed shared memories.

Dwg.6/7

Title Terms: DIRECTORY; LESS; MEMORY; ACCESS; PROTOCOL; METHOD; DISTRIBUTE; SHARE; MEMORY; COMPUTER; SYSTEM; TRANSFER; REQUEST; NODE; VALID; COPY; MEMORY; BLOCK; CAPABLE; SERVICE; ACCESS; REQUEST
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-013/14 ; G06F-015/16 ; G06F-015/167**
International Patent Class (Additional): **G06F-012/06**
File Segment: EPI

4/5/48 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638399 **Image available**
WPI Acc No: 1998-055307/199806
XRPX Acc No: N98-043811

Multiple threads access conflict preventing system - has storage facility associated with first dynamic lock structure for storing identities of third number of stored data objects

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E E; **HILL M D**
Number of Countries: 020 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 817040	A2	19980107	EP 97304516	A	19970625	199806	B
JP 10187527	A	19980721	JP 97187269	A	19970630	199839	
US 5835906	A	19981110	US 96673130	A	19960701	199901	

Priority Applications (No Type Date): US 96673130 A 19960701
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817040	A2	E	23	G06F-009/46	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10187527	A		22	G06F-012/00	
US 5835906	A			G06F-017/30	

Abstract (Basic): EP 817040 A

The system includes a dynamic lock structure having a number of dynamic lock structure elements, the number of which is fewer in number than a number of the first number of stored data objects. The mapping function renders it likely that only one stored data object of the second number of stored data objects that maps into the first dynamic lock structure member is accessed at any given point in time by a thread of the multiple threads.

A storage facility is associated with the first dynamic lock structure for storing identities of a third number of stored data objects. The latter represents a sub-set of the second number of stored data objects that are currently being accessed.

USE - For sharing stored data objects in computer system.

ADVANTAGE - Avoids access conflicts that may arise when multiple threads attempt to access same stored data object.

Dwg.3/6

Title Terms: MULTIPLE; THREAD; ACCESS; CONFLICT; PREVENT; SYSTEM; STORAGE; FACILITY; ASSOCIATE; FIRST; DYNAMIC; LOCK; STRUCTURE; STORAGE; IDENTIFY; THIRD; NUMBER; STORAGE; DATA; OBJECT
Derwent Class: T01
International Patent Class (Main): **G06F-009/46 ; G06F-012/00 ; G06F-017/30**
File Segment: EPI

4/5/49 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011409318 **Image available**
WPI Acc No: 1997-387225/199736
XRPX Acc No: N97-322334

Method of storing data in computer system with several coupled subsystems - involves storing data in computer system with several subsystems coupled to each other by system interconnect

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HAGERSTEN E; **WOOD D**
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

EP 780770	A1	19970625	EP 96309360	A	19961220	199736	B
JP 9185550	A	19970715	JP 96354752	A	19961220	199738	
US 5893144	A	19990406	US 95575787	A	19951222	199921	
SG 74576	A1	20000822	SG 9611749	A	19961217	200049	

Priority Applications (No Type Date): US 95575787 A 19951222
Cited Patents: 4.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 780770	A1	E	30	G06F-012/08	
Designated States (Regional): GB SE					
JP 9185550	A		28	G06F-012/08	
US 5893144	A			G06F-013/14	
SG 74576	A1			G06F-012/08	

Abstract (Basic): EP 780770 A

The method involves storing data in a computer system with several subsystems coupled to each other by a system interconnect. Each subsystem includes a processor, a hybrid non uniform memory architecture (NUMA COMA) cache, a COMA cache and a directory.

Data associated with a data line is stored in the hybrid NUMA COMA cache of one of the subsystems. It is determined whether the data should also be stored in the COMA cache of the one subsystem in a COMA mode.

USE/ADVANTAGE - Relates to hybrid caching architectures and protocols for multi-processor computer systems. Optimises COMA-only and NUMA-only caches architectures.

Dwg.3B/5

Title Terms: METHOD; STORAGE; DATA; COMPUTER; SYSTEM; COUPLE; SUBSYSTEM; STORAGE; DATA; COMPUTER; SYSTEM; SUBSYSTEM; COUPLE; SYSTEM; INTERCONNECT
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-013/14**
International Patent Class (Additional): **G06F-012/00 ; G06F-013/00**
File Segment: EPI

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Set     Items   Description
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             DAY D? OR FEEHRER, J? OR FEEHRER J? OR WOOD, D? OR WOOD D? OR
             PILLAI, P? OR PILLAI P? OR JACKSON, C? OR JACKSON C? OR HILL,
             M? OR HILL M?)
S2         34   S1 AND MEMORY()MANAGEMENT
S3         34   S2 NOT PY>2001
S4         34   S3 NOT PD>20011009
File   2:INSPEC 1969-2004/Mar W2
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Mar W3
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         (c) 2004 Inst for Sci Info
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         (c) 2004 ProQuest Info&Learning
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         (c) 1999 Information Handling Services
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         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Mar W1
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/Mar B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/Mar W2
         (c) 2004 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
         (c) 2004 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Apr
         (c) 2004 American Mathematical Society
File 275:Gale Group Computer DB(TM) 1983-2004/Mar 22
         (c) 2004 The Gale Group
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 647:CMP  Computer Fulltext 1988-2004/Mar W1
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/Mar W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Mar 19
         (c) 2004 The Dialog Corp.
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4/5,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4785149 INSPEC Abstract Number: C9411-6150J-028
Title: Kernel support for the Wisconsin Wind Tunnel
Author(s): Reinhardt, S.K.; Falsafi, B.; **Wood, D.A.**
Author Affiliation: Dept. of Comput. Sci., Wisconsin Univ., Madison, WI, USA
Conference Title: Proceedings of the USENIX Symposium on Microkernels and Other Kernel Architectures p.73-89
Publisher: USENIX Assoc, Berkeley, CA, USA
Publication Date: 1993 Country of Publication: USA 140 pp.
Conference Title: Proceedings of the USENIX Symposium on Microkernels and Other Kernel Architectures
Conference Date: 20-21 Sept. 1993 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: This paper describes a kernel interface that provides an untrusted user-level process (an executive) with protected access to **memory management** functions, including the ability to create, manipulate, and execute within subservient contexts (address spaces). Page motion callbacks not only give the executive limited control over physical **memory management** , but also shift certain responsibilities out of the kernel, greatly reducing kernel state and complexity. The executive interface was motivated by the requirements of the Wisconsin Wind Tunnel (WWT), a system for evaluating cache-coherent shared-memory parallel architectures. WWT uses the executive interface to implement a fine-grain user-level extension of Li's shared virtual memory on a Thinking Machines CM-5, a message-passing multicomputer. However, the interface is sufficiently general that an executive could act as a multiprogrammed operating system, exporting an alternative interface to the threads running in its subservient contexts. The executive interface is currently implemented as an extension to CMOST, the standard operating system for the CM-5. (16 Refs)
Subfile: C
Descriptors: message passing; operating systems (computers); parallel architectures; shared memory systems; storage management
Identifiers: page motion callbacks; kernel interface; untrusted user-level process; protected access; **memory management** functions; physical **memory management** ; executive interface; Wisconsin Wind Tunnel; cache-coherent shared-memory parallel architectures; fine-grain user-level extension; shared virtual memory; Thinking Machines CM-5; message-passing multicomputer; multiprogrammed operating system; threads; CMOST
Class Codes: C6150J (Operating systems); C6150N (Distributed systems); C6120 (File organisation)
Author(s): Reinhardt, S.K.; Falsafi, B.; **Wood, D.A.**
...Abstract: describes a kernel interface that provides an untrusted user-level process (an executive) with protected access to **memory management** functions, including the ability to create, manipulate, and execute within subservient contexts (address spaces). Page motion callbacks not only give the executive limited control over physical **memory management** , but also shift certain responsibilities out of the kernel, greatly reducing kernel state and complexity. The executive...
...Identifiers: **memory management** functions...

...physical **memory management** ;

4/5,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04256629 INSPEC Abstract Number: B9211-6230-013, C9211-5630-007
Title: Asynchronous transfer-mode receiver
Author(s): **Hill, M.** ; Cantoni, A.; Moors, T.

Author Affiliation: Dept. of Electr. & Electron. Eng., Univ. of Western Australia, Nedlands, WA, Australia

Journal: IEE Proceedings E (Computers and Digital Techniques) vol.139, no.5 p.401-9

Publication Date: Sept. 1992 Country of Publication: UK

CODEN: IPETD3 ISSN: 0143-7062

U.S. Copyright Clearance Center Code: 0143-7062/92/$3.00+0.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: Asynchronous cell-based transmission is the preferred transmission mode for emerging high-speed network standards such as the IEEE 802.6 metropolitan-area-network standard and the CCITT broadband integrated services digital network. These networks are envisaged to operate at bit rates in excess of 100 Mbit/s. The high bit rate and the cell-based mode of transmission pose challenging requirements on memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses a number of major generic issues addressed during the development. (15 Refs)

Subfile: B C

Descriptors: broadband networks; computer networks; ISDN; multiplexing equipment; standards; time division multiplexing

Identifiers: asynchronous transfer-mode receiver; cell-based transmission ; high-speed network standards; IEEE 802.6 metropolitan-area-network standard; CCITT broadband integrated services digital network; memory-buffer management; hardware architecture; **memory - management** techniques; packet-reassembly functions

Class Codes: B6230 (Switching centres and equipment); B6210L (Computer communications); B6210M (ISDN); C5630 (Networking equipment); C5620M (Metropolitan area networks)

Author(s): **Hill, M.** ; Cantoni, A.; Moors, T.

...Abstract: memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses...

...Identifiers: **memory - management** techniques

4/5,K/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

03605898 INSPEC Abstract Number: B90027504, C90026716

Title: A VLSI chip set for a multiprocessor workstation. II. A memory management **unit and cache controller**

Author(s): Jeong, D.-K.; **Wood, D.A.** ; Gibson, G.A.; Eggers, S.J.; Hodges, D.A.; Katz, R.H.; Patterson, D.A.

Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA

Journal: IEEE Journal of Solid-State Circuits vol.24, no.6 p. 1699-707

Publication Date: Dec. 1989 Country of Publication: USA

CODEN: IJSCBC ISSN: 0018-9200

U.S. Copyright Clearance Center Code: 0018-9200/89/1200-1699$01.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: For pt.I see ibid., vol.24, no.6, p.1688-98 (1989). The authors describe a **memory management** unit and a cache controller (MMU/CC) for a 40-70-MIPS multiprocessor workstation. The MMU/CC implements a novel **memory management** scheme, in-cache address translation, which does not require a translation lookaside buffer. It also implements a snooping bus protocol to maintain data consistency across all caches in the system. The chip is implemented in a 1.6- mu m double-layer-metal CMOS technology and

is being used in a multiprocessor workstation (SPUR) successfully executing a UNIX-like network-based operating system called Sprite as well as many applications, including LISP programs. (18 Refs)
Subfile: B C
Descriptors: buffer storage; CMOS integrated circuits; multiprocessing systems; storage management chips; VLSI; workstations
Identifiers: VLSI chip set; multiprocessor workstation; **memory management** unit; cache controller; in-cache address translation; snooping bus protocol; double-layer-metal; CMOS technology; SPUR; UNIX-like network-based operating system; Sprite; LISP programs; 1.6 micron; 40 to 70 MIPS
Class Codes: B1265Z (Other digital circuits); B1265D (Memory circuits); B2570D (CMOS integrated circuits); B1265F (Microprocessors and microcomputers); C5150 (Other circuits for digital computers); C5320G (Semiconductor storage); C5380 (Other aspects of storage devices and techniques); C5250 (Microcomputer techniques); C5440 (Multiprocessor systems and techniques)
Numerical Indexing: size 1.6E-06 m; computer execution rate 4.0E+07 to 7.0E+07 IPS

Title: A VLSI chip set for a multiprocessor workstation. II. A memory management **unit and cache controller**
Author(s): Jeong, D.-K.; **Wood, D.A.** ; Gibson, G.A.; Eggers, S.J.; Hodges, D.A.; Katz, R.H.; Patterson, D.A.
Abstract: For pt.I see ibid., vol.24, no.6, p.1688-98 (1989). The authors describe a **memory management** unit and a cache controller (MMU/CC) for a 40-70-MIPS multiprocessor workstation. The MMU/CC implements a novel **memory management** scheme, in-cache address translation, which does not require a translation lookaside buffer. It also implements a...
...Identifiers: **memory management** unit

4/5,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03326830 INSPEC Abstract Number: B89014916, C89019336
Title: The SPUR cache controller chip
Author(s): **Wood, D.A.** ; Eggers, S.J.; Gibson, G.A.; Deog-Kyoon Jeong; Katz, R.H.; Patterson, D.A.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: Southcon/88 Conference Record p.88-90
Publisher: Electron. Conventions Manage, Los Angeles, CA, USA
Publication Date: 1988 Country of Publication: USA iii+392 pp.
Conference Date: 8-10 March 1988 Conference Location: Orlando, FL, USA
Availability: Western Periodicals, North Hollywood, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The SPUR ('Symbolic Processing Using RISCs') Project is a research effort aimed at applying reduced instruction set computer concepts to the support of LISP programming environments. It extends previous Berkeley RISC efforts by exploring virtual memory, multiple processors, and co-processor support. The authors summarize the algorithms and implementation challenges of the cache controller chip. They briefly outline their protocol for cache coherency and mechanism for virtual **memory management** . They describe the on-chip performance monitoring hardware and some of the implementation challenges and solutions. Finally, the chip status and statistics are given. (4 Refs)
Subfile: B C
Descriptors: buffer storage; microprocessor chips; reduced instruction set computing; symbol manipulation
Identifiers: SPUR cache controller chip; Symbolic Processing; RISCs; LISP programming environments; protocol; cache coherency; virtual **memory management**
Class Codes: B1265F (Microprocessors and microcomputers); B1265D (Memory circuits); C5130 (Microprocessor chips); C5220 (Computer architecture);

C5320G (Semiconductor storage)

Author(s): **Wood, D.A.** ; Eggers, S.J.; Gibson, G.A.; Deog-Kyoon Jeong; Katz, R.H.; Patterson, D.A.

...Abstract: of the cache controller chip. They briefly outline their protocol for cache coherency and mechanism for virtual **memory management** . They describe the on-chip performance monitoring hardware and some of the implementation challenges and solutions. Finally...

...Identifiers: virtual **memory management**

4/5,K/5 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03565778 E.I. Monthly No: EI9303034633

Title: Asynchronous transfer mode receiver.

Author: **Hill, M.** ; Cantoni, A.; Moors, T.

Corporate Source: Curtin Univ of Technology, Perth, Aust

Source: IEE Proceedings, Part E: Computers and Digital Techniques v 139 n 5 Sep 1992 p 401-409

Publication Year: 1992

CODEN: IPETD3 ISSN: 0143-7062

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications)

Journal Announcement: 9303

Abstract: Asynchronous cell-based transmission is the preferred transmission mode for emerging high-speed network standards such as the IEEE 802.6 metropolitan area network standard and the CCITT broadband integrated services digital network. These networks are envisaged to operate at bit rates in excess of 100 Mbit/s. The high bit rate and the cell-based mode of transmission pose challenging requirements on memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses a number of major generic issues addressed during the development. (Author abstract) 15 Refs.

Descriptors: *METROPOLITAN AREA NETWORKS; STANDARDS; VOICE/DATA COMMUNICATION SYSTE; DIGITAL COMMUNICATION SYSTEMS; DATA STORAGE EQUIPMENT; COMPUTER ARCHITECTURE; SIGNAL RECEIVERS

Identifiers: TRANSFER MODE RECEIVERS; ASYNCHRONOUS TRANSMISSION; IEEE STANDARDS; CCITT STANDARDS; INTEGRATED SERVICE DIGITAL NETWORKS; MEMORY-BUFFER MANAGEMENT

Classification Codes:

722 (Computer Hardware); 716 (Radar, Radio & TV Electronic Equipment); 902 (Engineering Graphics & Standards)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 90 (GENERAL ENGINEERING)

Author: **Hill, M.** ; Cantoni, A.; Moors, T.

...Abstract: memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses...

4/5,K/6 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02891818 E.I. Monthly No: EIM9004-016501

Title: VLSI chip set for a multiprocessor workstation - II: A memory management **unit and cache controller.**

Author: Jeong, Deog-Kyoon; **Wood, David A.** ; Gibson, Garth A.; Eggers, Susan J.; Hodges, David A.; Katz, Randy H.; Patterson, David A.
Corporate Source: Univ of California, Dep of Electr Eng & Comput Sci, Berkeley, CA, USA
Conference Title: International Solid-State Circuits Conference
Conference Location: USA Conference Date: 19890200
E.I. Conference No.: 13038.
Source: IEEE Journal of Solid-State Circuits v 24 n 6 Dec 1989. p 1699-1707
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 9004
Abstract: The authors describe a **memory management** unit and a cache controller (MMU/CC) for a 40-70-MIPS multiprocessor workstation. The MMU/CC implements a novel **memory management** scheme, in-cache address translation, which does not require a translation lookaside buffer. It also implements a snooping bus protocol to maintain data consistency across all caches in the system. The chip is implemented in a 1.6- mu m double-layer-metal CMOS technology and is being used in a multiprocessor workstation (SPUR) successfully executing a UNIX-like network-based operating system called Sprite as well as many applications, including LISP programs. 18 Refs.
Descriptors: *DATA STORAGE, DIGITAL--*Control; COMPUTER SYSTEMS, DIGITAL --Multiprocessing; COMPUTER OPERATING SYSTEMS; INTEGRATED CIRCUITS, VLSI
Identifiers: CACHE CONTROLLER; **MEMORY MANAGEMENT** UNIT; MULTIPROCESSOR WORKSTATION; SNOOPING BUS PROTOCOL; CMOS INTEGRATED CIRCUIT; OPERATING SYSTEM SPRITE
Classification Codes:
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 723 (Computer Software); 713 (Electronic Circuits); 714 (Electronic Components)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

Title: VLSI chip set for a multiprocessor workstation - II: A memory management **unit and cache controller.**
Author: Jeong, Deog-Kyoon; **Wood, David A.** ; Gibson, Garth A.; Eggers, Susan J.; Hodges, David A.; Katz, Randy H.; Patterson, David A.
Abstract: The authors describe a **memory management** unit and a cache controller (MMU/CC) for a 40-70-MIPS multiprocessor workstation. The MMU/CC implements a novel **memory management** scheme, in-cache address translation, which does not require a translation lookaside buffer. It also implements a...
Identifiers: CACHE CONTROLLER; **MEMORY MANAGEMENT** UNIT; MULTIPROCESSOR WORKSTATION; SNOOPING BUS PROTOCOL; CMOS INTEGRATED CIRCUIT; OPERATING SYSTEM SPRITE

4/5,K/7 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00100716 E.I. Monthly No: EI70X145060
Title: Measurements of segment size.
Author: BATSON, A.; JU, S. M.; **WOOD, D. C.**
Corporate Source: Univ of Virginia, Charlottesville
Source: Commun ACM v 13 n 3 Mar 1970 p 155-9
Publication Year: 1970
Language: ENGLISH
Journal Announcement: 70X1
Abstract: Distributions of segment sizes measured under routine operating conditions on a computer system which utilizes variable sized segments (the Burroughs B5500) are discussed. The most striking feature of the measurements is the large number of small segments- about 60% of the segments in use contain less than 40 words. Although the results are certainly not installation independent, and although they are particularly influenced by features of the B5500 ALGOL system, they should be relevant

to the design of new computer systems, especially with respect to the organization of paging schemes.
Descriptors: *COMPUTERS--*Operating Systems
Identifiers: DYNAMIC **MEMORY** **MANAGEMENT**
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

Author: BATSON, A.; JU, S. M.; **WOOD**, **D. C.**
Identifiers: DYNAMIC **MEMORY** **MANAGEMENT**

4/5,K/8 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

07645855 Genuine Article#: 191EF Number of References: 52
Title: Cache-conscious structure layout
Author(s): Chilimbi TM (REPRINT) ; **Hill MD** ; Larus JR
Corporate Source: UNIV WISCONSIN,DEPT COMP SCI, 1210 W DAYTON ST/MADISON//WI/53706 (REPRINT); MICROSOFT CORP,RES/REDMOND//WA/98052
Journal: ACM SIGPLAN NOTICES, 1999, V34, N5 (MAY), P1-12
ISSN: 0362-1340 Publication date: 19990500
Publisher: ASSOC COMPUTING MACHINERY, 1515 BROADWAY, NEW YORK, NY 10036
Language: English Document Type: ARTICLE
Geographic Location: USA
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: COMPUTER SCIENCE, SOFTWARE, GRAPHICS, PROGRAMMING
Abstract: Hardware trends have produced an increasing disparity between processor speeds and memory access times. While a variety of techniques for tolerating or reducing memory latency have been proposed, these are rarely successful for pointer-manipulating programs.

This paper explores a complementary approach that attacks the source (poor reference locality) of the problem rather than its manifestation (memory latency). It demonstrates that careful data organization and layout provides an essential mechanism to improve the cache locality of pointer-manipulating programs and consequently, their performance. It explores two placement techniques-clustering and coloring-that improve cache performance by increasing a pointer structure's spatial and temporal locality, and by reducing cache-conflicts.

To reduce the cost of applying these techniques, this paper discusses two strategies-cache-conscious reorganization and cache-conscious allocation-and describes two semi-automatic tools-ccmorph and ccmalloc-that use these strategies to produce cache-conscious pointer structure layouts. ccmorph is a transparent tree reorganizer that utilizes topology information to cluster and color the structure. ccmalloc is a cache-conscious heap allocator that attempts to co-locate contemporaneously accessed data elements in the same physical cache block. Our evaluations, with microbenchmarks, several small benchmarks, and a couple of large real-world applications, demonstrate that the cache-conscious structure layouts produced by,ccmorph and ccmalloc offer large performance benefits-in most cases, significantly outperforming state-of-the-art prefetching.
Descriptors--Author Keywords: cache-conscious data placement ; clustering ; coloring ; cache-conscious allocation ; cache-conscious reorganization
Identifiers--KeyWord Plus(R): **MEMORY** **MANAGEMENT** ; LOCALITY; MODEL
Cited References:
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WOLF ME, 1991, V26, P30, SIGPLAN NOTICES

Author(s): Chilimbi TM (REPRINT) ; **Hill MD** ; Larus JR
...Identifiers-- **MEMORY MANAGEMENT** ; LOCALITY; MODEL

4/5,K/9 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02001028 Genuine Article#: JT467 Number of References: 15
Title: ASYNCHRONOUS TRANSFER MODE RECEIVER
Author(s): **HILL M** ; CANTONI A; MOORS T
Corporate Source: CURTIN UNIV TECHNOL,AUSTRALIAN TELECOMMUN RES INST,GPO BOX U 1987/PERTH/WA 6001/AUSTRALIA/
Journal: IEE PROCEEDINGS-E COMPUTERS AND DIGITAL TECHNIQUES, 1992, V139, N5 (SEP), P401-409
ISSN: 0143-7062
Language: ENGLISH Document Type: ARTICLE
Geographic Location: AUSTRALIA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: COMPUTER APPLICATIONS & CYBERNETICS

Abstract: Asynchronous cell-based transmission is the preferred transmission mode for emerging high-speed network standards such as the IEEE 802.6 metropolitan area network standard and the CCITT broadband integrated services digital network. These networks are envisaged to operate at bit rates in excess of 100 Mbit/s. The high bit rate and the cell-based mode of transmission pose challenging requirements on memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses a number of major generic issues addressed during the development.

Descriptors--Author Keywords: NETWORKS ; **MEMORY MANAGEMENT** ; PACKET SWITCHING ; ASYNCHRONOUS TRANSFER MODE (ATM) ; PACKET REASSEMBLY

Research Fronts: 90-7830 001 (OPTICAL FIBER METROPOLITAN-AREA NETWORKS; WAVELENGTH DIVISION MULTIPLE ACCESS; MULTIMEDIA SYSTEMS)

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Author(s): **HILL M** ; CANTONI A; MOORS T

...Abstract: memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses...

4/5,K/10 (Item 3 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

00014802 Genuine Article#: CE692 Number of References: 19

Title: A VLSI CHIP SET FOR A MULTIPROCESSOR WORKSTATION .2. - A MEMORY MANAGEMENT **UNIT AND CACHE CONTROLLER**

Author(s): JEONG DK; **WOOD DA** ; GIBSON GA; EGGERS SJ; HODGES DA; KATZ RH; PATTERSON DA

Corporate Source: TEXAS INSTRUMENTS INC/DALLAS//TX/75265; UNIV CALIF BERKELEY,DEPT ELECT ENGN & COMP SCI/BERKELEY//CA/94720

Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1989, V24, N6, P1699-1707

Language: ENGLISH Document Type: ARTICLE

Geographic Location: USA

Subfile: SciSearch; Scisearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences

Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC

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JEONG DK, 1987, V22, P255, IEEE J SOLID-ST CIRC
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WOOD DA, IN PRESS IEEE DESIGN
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WOOD DA, 1989, UCBCSD89490 U CAL CO
WOOD DA, 1986, P358, 13TH P ANN S COMP AR

Title: A VLSI CHIP SET FOR A MULTIPROCESSOR WORKSTATION .2. - A MEMORY MANAGEMENT **UNIT AND CACHE CONTROLLER**
Author(s): JEONG DK; **WOOD DA** ; GIBSON GA; EGGERS SJ; HODGES DA; KATZ RH; PATTERSON DA

4/5,K/11 (Item 1 from file: 95)

01078059 E96070791259
Decoupled hardware support for distributed shared memory
(Entkopplte Hardwareunterstuetzung fuer gemeinsam genutzte verteilte Speicher)
Reinhardt, SK; Pfile, RW; **Wood, DA**
Univ. of Wisconsin-Madison, Madison, USA
Computer Architecture News, v24, n2, pp34-43, 1996
Document type: journal article Language: English
Record type: Abstract
ISSN: 0163-5964

ABSTRACT:
This paper investigates hardware support for fine-grain distributed shared memory (DSM) in networks of workstations. To reduce design time and implementation cost relative to dedicated DSM systems, the authors decouple the functional hardware components of DSM support, allowing greater used of off-the-shelf devices. They present two decoupled systems, Typhoon-0 and Typhoon-1. Typhoon-0 uses an off-the-shelf protocal processor and network interface; a custom access control device is the only DSM-specific hardware. To demonstrate the feasibility and simplicity of the access control device, they designed and built an FPGA-based version in under one year. Typhoon-1 also uses on off-the-shelf protocol processor, but integrates the network interface and access control devices for higher performance. They compare the two decoupled systems with two integrated systems via simulation. For six benchmarks on 32 nodes, Typhoon-0 ranges from 30 % to 309 % slower than the best integrated system, while Typhoon-1 ranges from 13 % to 132 % slower. Four of the six benchmarks achieve speedups of 12 to 18 on Typhoon-0 and 15 to 26 on Typhoon-1, compared with 19 to 35 on the best integrated system. Two benchmarks are hampered by high communication overheads, but selectively replacing shared-memory operations with message passing provides speedups of at least 16 on both decoupled systems. These speedups indicate that decoupled designs can potentially provide a cost-effective alternative to complex high-end DSM systems.

DESCRIPTORS: LOCAL COMPUTER NETWORKS; **MEMORY MANAGEMENT** ; WORK STATIONS; SYSTEMS DESIGN; IMPLEMENTATION; COMMUNICATION PROTOCOLS; SIGNAL PROCESSING EQUIPMENT; COMPUTER INTERFACES; MODEL SIMULATION; PERFORMANCE EVALUATION; BENCHMARKING
IDENTIFIERS: Workstationnetzwerk; gemeinsamer Speicher; Hardwareloesung

Reinhardt, SK; Pfile, RW; **Wood, DA**
DESCRIPTORS: LOCAL COMPUTER NETWORKS; **MEMORY MANAGEMENT** ; WORK STATIONS; SYSTEMS DESIGN; IMPLEMENTATION; COMMUNICATION PROTOCOLS; SIGNAL PROCESSING

EQUIPMENT; COMPUTER INTERFACES; MODEL SIMULATION; PERFORMANCE EVALUATION; BENCHMARKING

4/5,K/12 (Item 2 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

01078041 E96070810259
Coherent network interfaces for fine-grain communication
(Kohaerente Netzwerkschnittstellen fuer feingranulare Kommunikation)
Mukherjee, SS; Babak Falsafi; **Hill, MD ; Wood, DA**
Univ. of Wisconsin-Madison, Madison, USA
Computer Architecture News, v24, n2, pp247-258, 1996
Document type: journal article Language: English
Record type: Abstract
ISSN: 0163-5964

ABSTRACT:
Historically, processor accesses to memory-mapped device registers have been marked uncachable to insure their visibility to the device. The ubiquity of snooping cache coherence, however, makes it possible for processors and devices to interact with cachable, coherent memory operations. Using coherence can improve performance by facilitating burst transfers of whole cache blocks and reducing control overheads (e.g., for polling). This paper begins on exploration of network interfaces (NIs) that use coherence - coherent network interfaces (CNIs) - to improve communication performance. The authors restrict this study to NI/CNIs that reside on coherent memory or I/O buses, to NI/CNIs that are much simpler than processors, and to the performance of fine-grain messaging from user process to user process. Their first contribution is to develop and optimize two mechanisms that CNIs use to communicate with processors. A cachable device register - derived from cachable control registers - is a coherent, cachable block of memory used to transfer status, control, or data between a device and a processor. Cachable queues generalize cachable device registers from one cachable, coherent memory block to a contiguous region of cachable, coherent blocks managed as a circular queue. Their second contribution is a taxonomy and comparison of four CNIs with a more conventional NI. Microbenchmark results show that CNIs can improve the round-trip latency and achievable bandwidth of a small 64-byte message by 37 % and 125 % respectively on the memory bus and 74 % and 123 % respectively on a coherent I/O bus. Experiments with five macrobenchmarks show that CNIs can improve the performance by 17-53 % on the memory bus and 30-88 % on the I/O bus.

DESCRIPTORS: INTERCONNECTION NETWORKS--CIRCUITS; MULTICOMPUTER SYSTEMS; MULTIPROCESSING SYSTEMS; **MEMORY MANAGEMENT** ; CACHE MEMORIES; DATA COMMUNICATION; BENCHMARKING; COMPUTER INTERFACES; DATA BUS; COMPUTER PERFORMANCE; PERFORMANCE EVALUATION
IDENTIFIERS: Mehrprozessorsystem; kohaerente Netzwerkschnittstelle
Mukherjee, SS; Babak Falsafi; **Hill, MD ; Wood, DA**
...DESCRIPTORS: CIRCUITS; MULTICOMPUTER SYSTEMS; MULTIPROCESSING SYSTEMS; **MEMORY MANAGEMENT** ; CACHE MEMORIES; DATA COMMUNICATION; BENCHMARKING; COMPUTER INTERFACES; DATA BUS; COMPUTER PERFORMANCE; PERFORMANCE EVALUATION

4/5,K/13 (Item 3 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00896440 E95066535031
Paging tradeoffs in distributed-shared-memory multiprocessors
(Ueber das Paging von Tradeoffs in verteilten Multiprozessorumgebungen mit gemeinsamem Speicher)
Burger, DC; Hyder, RS; Miller, BP; **Wood, DA**
Univ. of Wisconsin, Madison, USA
1994 Supercomputing Conf., Proc., Washington, USA, Nov 14-18, 19941994

Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8186-6607-2

ABSTRACT:
Massively parallel processors have begun using commodity operating systems that support demand-paged virtual memory. To evaluate the utility of virtual memory, the authors measured the behavior of seven shared-memory parallel application programs on a simulated distributed shared-memory machine. The results (i) confirm the importance of gang CPU scheduling, (ii) show that a page-faulting processor should spin rather than invoke a parallel context switch, (iii) show that the parallel programs frequently touch most of their data, and (iv) indicate that memory, not just CPUs, must be 'gang scheduled'. Overall, the experiments demonstrate that demand paging has limited value on concurrent parallel machines because of the applications' synchronization and memory reference patterns and the machines' high page-fault and parallel-context-switch overhead.

DESCRIPTORS: MULTIPROCESSING SYSTEMS; **MEMORY MANAGEMENT** ; DISTRIBUTED PARAMETER SYSTEMS; DISTRIBUTED COMPUTING; PARALLEL PROCESSING; PARALLEL PROCESSORS
IDENTIFIERS: TRADEOFF; Paging; Tradeoffs; Shared-Memory; verteilte Multiprocessoren

Burger, DC; Hyder, RS; Miller, BP; **Wood, DA**
DESCRIPTORS: MULTIPROCESSING SYSTEMS; **MEMORY MANAGEMENT** ; DISTRIBUTED PARAMETER SYSTEMS; DISTRIBUTED COMPUTING; PARALLEL PROCESSING; PARALLEL PROCESSORS

4/5,K/14 (Item 4 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00888814 I95045645259
An interface to a reliable packet delivery service for parallel systems
(Eine Schnittstelle fuer einen zuverlaessigen Paketuebergabedienst fuer Parallelsysteme)
Debbage, M; **Hill, MB** ; Nicole, DA
Archit. Group, INMOS Ltd., Bristol, UK
IEEE Transactions on Parallel and Distributed Systems, v6, n4, pp400-411, 1995
Document type: journal article Language: English
Record type: Abstract
ISSN: 1045-9219

ABSTRACT:
Modern distributed memory parallel computers provide hardware support for the efficient and reliable delivery of interprocessor messages. This facility needs to be accessed by lightweight protocols that do not waste the performance of the underlying hardware; the heavyweight layering techniques traditionally used in distributed systems are wholly inappropriate. A low-level communication interface is therefore presented which exploits modern architectures effectively, while maintaining a good match to existing parallel programming environments. The interface defines mechanisms to access an asynchronous reliable packet delivery service. It permits messaging protocols to be efficiently synthesized by considering the activity at their end-points alone. This arrangement effectively decouples the implementation of protocols from low-level architectural features, and hence aids the portability of parallel programming environments. Furthermore, the interface allows the communication network to be shared by multiple programming paradigms, giving additional flexibility over existing systems.

DESCRIPTORS: COMPUTER INTERFACES; PACKET SWITCHING; PARALLEL PROGRAMMING; PROGRAMMING ENVIRONMENTS; COMMUNICATION PROTOCOLS; PORTABILITY--SOFTWARE; PARALLEL PROCESSING; **MEMORY MANAGEMENT** ; COMPUTER ARCHITECTURE

IDENTIFIERS: RELIABLE PACKET DELIVERY SERVICE INTERFACE; PARALLEL SYSTEMS; DISTRIBUTED MEMORY PARALLEL COMPUTERS; INTERPROCESSOR MESSAGES; LIGHTWEIGHT PROTOCOLS; HEAVYWEIGHT LAYERING TECHNIQUES; LOW LEVEL COMMUNICATION INTERFACE; PARALLEL PROGRAMMING ENVIRONMENTS; MESSAGING PROTOCOLS; LOW LEVEL ARCHITECTURAL FEATURES; Parallelverarbeitung; Uebergabeprotokoll

Debbage, M; **Hill, MB** ; Nicole, DA
...DESCRIPTORS: SOFTWARE; PARALLEL PROCESSING; **MEMORY MANAGEMENT** ; COMPUTER ARCHITECTURE

4/5,K/15 (Item 5 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00853042 E95026082046
Fine-grain access control for distributed shared memory
(Feinkoernige Zugriffssteuerung fuer einen verteilten gemeinsamen Speicher)
Schoinas, I; Falsafi, B; Lebeck, AR; Reinhardt, SK; Larus, JR; **Wood, DA**
Univ. of Wisconsin, Madison, USA
ASPLOS-VI, Proc., 6th Int. Conf. on Architectural Support for Programming Languages and Operating Syst., San Jose, USA, Oct 4-7, 19941994
Document type: journal article Language: English
Record type: Abstract

ABSTRACT:
This paper discusses implementations of fine-grain memory access control, which selectively restricts reads and writes to cache-block-sized memory regions. Fine-grain access control forms the basis of efficient cache-coherent shared memory. This paper focuses on low-cost implementations that require little or no additional hardware. These techniques permit efficient implementation of shared memory on a wide range of parallel systems, thereby providing shared-memory codes with a portability previously limited to message passing. This paper categorizes techniques based on where access control is enforced and where access conflicts are handled. The authors incorporated three techniques that require no additional hardware into Blizzard, a system that supports distributed shared memory on the CM-5. The first adds a software lookup before each shared-memory reference by modifying the program's executable. The second uses the memory's error correcting code (ECC) as cache-block valid bits. The third is a hybrid. The software technique ranged from slightly faster to two times slower than the ECC approach. Blizzard's performance is roughly comparable to a hardware shared-memory machine. These results argue that clusters of workstations or personal computers with networks comparable to the CM-5's will able to support the same shared-memory interfaces as supercomputers.

DESCRIPTORS: ACCESS; **MEMORY MANAGEMENT** ; CACHE MEMORIES; IMPLEMENTATION; MASSIVELY PARALLEL MACHINES; PARALLEL PROCESSING; COMPUTER INTERFACES; PORTABILITY--SOFTWARE; COMPUTER NETWORKS; DISTRIBUTED COMPUTING; PERFORMANCE EVALUATION
IDENTIFIERS: ZUGRIFFSSTEUERUNG; GEMEINSAMER SPEICHER; CACHE KOHAERENZ; verteilter gemeinsamer Speicher; Zugriffssteuerung

Schoinas, I; Falsafi, B; Lebeck, AR; Reinhardt, SK; Larus, JR; **Wood, DA**
DESCRIPTORS: ACCESS; **MEMORY MANAGEMENT** ; CACHE MEMORIES; IMPLEMENTATION; MASSIVELY PARALLEL MACHINES; PARALLEL PROCESSING; COMPUTER INTERFACES; PORTABILITY...

4/5,K/16 (Item 6 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00734511 I93115172205
A unified formalization of four shared-memory models
(Eine vereinheitlichte Formalisierung von vier Modellen der gemeinsamen

Speicherbenutzung)
Adve, SV; **Hill, MD**
Dept. of Comput. Sci., Wisconsin Univ., Madison, WI, USA
IEEE Transactions on Parallel and Distributed Systems, v4, n6, pp613-624, 1993
Document type: journal article Language: English
Record type: Abstract
ISSN: 1045-9219

ABSTRACT:
The authors present a data-race-free-1, shared-memory model that unifies four earlier models: weak ordering, release consistency (with sequentially consistent special operations), the VAX memory model, and data-race-free-0. Data-race-free-1 unifies the models of weak ordering, release consistency, the VAX, and data-race-free-0 by formalizing the intuition that if programs synchronize explicitly and correctly, then sequential consistency can be guaranteed with high performance in a manner that retains the advantages of each of the four models. Data-race-free-1 expresses the programmer's interface more explicitly and formally than weak ordering and the VAX, and allows an implementation not allowed by weak ordering, release consistency, or data-race-free-0. The implementation proposal for data-race-free-1 differs from earlier implementations by permitting the execution of all synchronization operations of a processor even while previous data operations of the processor are in progress. To ensure sequential consistency, two sychronizing processors exchange information to delay later operations of the second processor that conflict with an incomplete data operation of the first processor.

DESCRIPTORS: **MEMORY MANAGEMENT** ; PARALLEL PROCESSING; SYSTEM ARCHITECTURE; DATA MEMORY; MULTICOMPUTER SYSTEMS; SHARED MEMORY SYSTEMS
IDENTIFIERS: MULTIPROCESSORS; HAZARDS AND RACE CONDITIONS; FORMALIZATION; SHARED MEMORY MODELS; WEAK ORDERING; RELEASE CONSISTENCY; SEQUENTIAL CONSISTENCY; gemeinsamer Speicher; Parallelarchitektur

Adve, SV; **Hill, MD**
DESCRIPTORS: **MEMORY MANAGEMENT** ; PARALLEL PROCESSING; SYSTEM ARCHITECTURE; DATA MEMORY; MULTICOMPUTER SYSTEMS; SHARED MEMORY SYSTEMS

4/5,K/17 (Item 7 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00621534 I92114279928
Asynchronous transfer-mode receiver
(Asynchroner Datenuebertragungsempfaenger fuer auf Zellstruktur basierende Datenpaketuebertragung in Hochgeschwindigkeitsrechnernetzen)
Hill, M ; Cantoni, A; Moors, T
Dept. of Electr. & Electron. Eng., Univ. of Western Australia, Nedlands, WA, Australia
IEE Proceedings, Part E (Computers and Digital Techniques), v139, n5, pp401-409, 1992
Document type: journal article Language: English
Record type: Abstract
ISSN: 0143-7062

ABSTRACT:
Asynchronous cell-based transmission is the preferred transmission mode for emerging high-speed network standards such as the IEEE 802.6 metropolitan-area-network standard and the CCITT broadband integrated services digital network. These networks are envisaged to operate at bit rates in excess of 100 Mbit/s. The high bit rate and the cell-based mode of transmission pose challenging requirements on memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed

asynchronous-transfer-mode-based network. The paper also discusses a number of major generic issues addressed during the development.

DESCRIPTORS: BROADBAND NETWORKS; COMPUTER NETWORKS; MULTIPLEXERS; STANDARDS ; TEMPORAL MULTIPLEXING; BRANCH POINTS; DATA RECEIVER; ASYNCHRONOUS OPERATION; PACKET SWITCHING; INTEGRATED SERVICES DIGITAL NETWORKS
IDENTIFIERS: HARDWARE ARCHITECTURE; ASYNCHRONOUS TRANSFER MODE RECEIVER; CELL BASED TRANSMISSION; HIGH SPEED NETWORK STANDARDS; CCITT BROADBAND INTEGRATED SERVICES DIGITAL NETWORK; MEMORY BUFFER MANAGEMENT; **MEMORY MANAGEMENT** TECHNIQUES; PACKET REASSEMBLY FUNCTIONS; MAN--(METROPOLITAN AREA NETWORK); Asynchronempfaenger; Breitbandrechnernetz; Knoten

Hill, M; Cantoni, A; Moors, T

ABSTRACT:
...memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discusses...
...IDENTIFIERS: RECEIVER; CELL BASED TRANSMISSION; HIGH SPEED NETWORK STANDARDS; CCITT BROADBAND INTEGRATED SERVICES DIGITAL NETWORK; MEMORY BUFFER MANAGEMENT; **MEMORY MANAGEMENT** TECHNIQUES; PACKET REASSEMBLY FUNCTIONS; MAN...

4/5,K/18 (Item 8 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00615505 E92103213025
Sorting, measures of disorder, and worst-case performance
(Sortierung, Messung der Unordnung und Leistung unter schlechtester Bedingung)
Estivill-Castro, V; **Wood, D**
York Univ., CDN; Univ. of Waterloo, CDN
New Results and New Trends in Computer Science, Graz, A, June 20-21, 1991
1991
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 3-540-54869-6; 0-387-54869-6

ABSTRACT:
We design main memory algorithms that sort in worst-case time such that the time varies smoothly from linear to optimal time for files that vary from being nearly sorted and have little disorder to being very unsorted. They are adaptive sorting algorithms. To this end, we: A) introduce three basic ways of measuring nearly sortedness or disorder; B) give a sorting algorithm, Strip Sort, that is worst-case-optimally adaptive to one of them; C) give an axiomatic definition of measures of disorder; D) and provide an infinitude of sorting algorithms that can be proved to be adaptive, with respect to many different measures, under some reasonable assumptions.

DESCRIPTORS: ALGORITHM; **MEMORY MANAGEMENT** ; WORST CASES; SELECTION--SORTING; IMPROVEMENT; DATA MEMORY; DATA STORAGE
IDENTIFIERS: Speicherverwaltung; Algorithmus

Estivill-Castro, V; **Wood, D**
DESCRIPTORS: ALGORITHM; **MEMORY MANAGEMENT** ; WORST CASES; SELECTION...

4/5,K/19 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1193492 H.W. WILSON RECORD NUMBER: BAST94062137

Cache profiling and the SPEC benchmarks: a case study
Lebeck, Alvin R; **Wood, David A**
Computer v. 27 (Oct. '94) p. 15-26
DOCUMENT TYPE: Feature Article ISSN: 0018-9162 LANGUAGE: English
RECORD STATUS: New record

ABSTRACT: As VLSI technology improvements continue to widen the gap between processor and main memory cycle times, cache performance becomes increasingly important to overall system performance. Cache memories help alleviate the cycle-time disparity, although only for programs that exhibit sufficient spatial and temporal locality. Programs with unruly access patterns consume a lot of time transferring data to and from the cache. To fully exploit the performance potential of fast processors, programmers must explicitly consider cache behavior, restructuring their codes to increase locality. As these fast processors proliferate, techniques for improving cache performance must move beyond the supercomputer and multiprocessor communities and into the mainstream of computing. In this article, the authors examine some of the techniques programmers can use to improve cache performance. They show how to use CProf, a cache profiler, to identify cache performance bottlenecks and gain insight into their origin. This insight helps programmers understand which of the well-known program transformations are likely to improve cache performance. Using CProf and simple transformations, they show how to tune the cache performance of six of the SPEC92 benchmarks. By restructuring the source code, the benchmarks greatly improve cache behavior and achieve execution time speedups ranging from 1.02 to 3.46. The speedup depends on the machine's memory system, with greater speedups obtained in the Fortran programs.

DESCRIPTORS: Cache memory devices; Benchmark problems; **Memory management** (Computer science);

Wood, David A

DESCRIPTORS: ... **Memory management** (Computer science) ;

4/5,K/20 (Item 2 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1057591 H.W. WILSON RECORD NUMBER: BAST92056382
Asynchronous transfer mode receiver
Hill, M ; Cantoni, A; Moors, T
IEE Proceedings. Part E, Computers and Digital Techniques v. 139 (Sept. '92) p. 401-9
DOCUMENT TYPE: Feature Article ISSN: 0143-7062 LANGUAGE: English
RECORD STATUS: New record

DESCRIPTORS: **Memory management** (Computer science); Asynchronous transfer mode; CCITT standards;

Hill, M ;

DESCRIPTORS: **Memory management** (Computer science...
;

4/5,K/21 (Item 3 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

0878788 H.W. WILSON RECORD NUMBER: BAST90004955
A VLSI chip set for a multiprocessor workstation: a memory management **unit and cache controller**
Jeong, Deog-Kyoon; **Wood, David A** ; Gibson, Garth A
IEEE Journal of Solid-State Circuits v. 24 (Dec. '89) p. 1699-707

DOCUMENT TYPE: Feature Article ISSN: 0018-9200 LANGUAGE: English
RECORD STATUS: New record

DESCRIPTORS: Cache memory devices; Workstations--Design; **Memory management** (Computer science);

A VLSI chip set for a multiprocessor workstation: a memory management **unit and cache controller**
Wood, David A ...

DESCRIPTORS: ... **Memory management** (Computer science) ;

4/5,K/22 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

03877448 EDB-95-121216
Title: Paging tradeoffs in distributed-shared-memory multiprocessors
Author(s): Burger, D.C.; Hyder, R.S.; Miller, B.P.; **Wood, D.A.** (Univ. of Wisconsin, Madison, WI (United States). Computer Sciences Dept.)
Title: Supercomputing '94: Proceedings
Conference Title: Supercomputing '94 meeting
Conference Location: Washington, DC (United States) Conference Date: 14-18 Nov 1994
Publisher: Los Alamitos, CA (United States) IEEE Computer Society Press
Publication Date: 1994
p 590-599 (849 p)
Report Number(s): CONF-941118--
Contract Number (DOE): FG02-93ER25176
ISBN: 0-8186-6605-6
Document Type: Analytic of a Book; Conference Literature; Numerical Data
Language: English
Journal Announcement: EDB9518
Availability: IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331 (United States) $170.00
Subfile: ERA (Energy Research Abstracts); ETD (Energy Technology Data Exchange). IMS (DOE contractor)
US DOE Project/NonDOE Project: P
Country of Origin: United States
Country of Publication: United States
Abstract: Massively parallel processors have begun using commodity operating systems that support demand-paged virtual memory. To evaluate the utility of virtual memory, the authors measured the behavior of seven shared memory parallel application programs on a simulated distributed-shared-memory machine. The results (1) confirm the importance of gang CPU scheduling, (2) show that a page-faulting processor should spin rather than invoke a parallel context switch, (3) show that the parallel programs frequently touch most of their data, and (4) indicate that memory, not just CPUs, must be gang scheduled''. Overall, the experiments demonstrate that demand paging has limited value on current parallel machines because of the applications' synchronization and memory reference patterns and the machines' high page-fault and parallel-context-switch overheads.
Major Descriptors: SUPERCOMPUTERS -- **MEMORY MANAGEMENT** ; *SUPERCOMPUTERS -- TASK SCHEDULING
Descriptors: DISTRIBUTED DATA PROCESSING; EXECUTIVE CODES; EXPERIMENTAL DATA; PARALLEL PROCESSING; USES
Broader Terms: COMPUTER CODES; COMPUTERS; DATA; DATA PROCESSING; DIGITAL COMPUTERS; INFORMATION; NUMERICAL DATA; PROCESSING; PROGRAMMING
Subject Categories: 990200* -- Mathematics & Computers

...Author(s): **Wood, D.A.** (Univ. of Wisconsin, Madison, WI (United States). Computer Sciences Dept.)
Major Descriptors: SUPERCOMPUTERS -- **MEMORY MANAGEMENT** ; *

.4/5,K/23 **(Item 2 from file: 103)**
DIALOG(R)File 103:Energy SciTec

03877430 EDB-95-121198
Title: Application-specific protocols for user-level shared memory
Author(s): Falsafi, B.; Lebeck, A.R.; Reinhardt, S.K.; Schoinas, I.; **Hill, M.D.** ; Larus, J.R.; Rogers, A.; **Wood, D.A.** (Univ. of Wisconsin, Madison, WI (United States). Computer Sciences Dept.)
Title: Supercomputing '94: Proceedings
Conference Title: Supercomputing '94 meeting
Conference Location: Washington, DC (United States) Conference Date: 14-18 Nov 1994
Publisher: Los Alamitos, CA (United States) IEEE Computer Society Press
Publication Date: 1994
p 380-389 (849 p)
Report Number(s): CONF-941118--
ISBN: 0-8186-6605-6
Document Type: Analytic of a Book; Conference Literature
Language: English
Journal Announcement: EDB9518
Availability: IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331 (United States) $170.00
Subfile: ERA (Energy Research Abstracts); ETD (Energy Technology Data Exchange). IMS (DOE contractor)
US DOE Project/NonDOE Project: NP
Country of Origin: United States
Country of Publication: United States
Abstract: Recent distributed shared memory (DSM) systems and proposed shared-memory machines have implemented some or all of their cache coherence protocols in software. One way to exploit the flexibility of this software is to tailor a coherence protocol to match an application's communication patterns and memory semantics. This paper presents evidence that this approach can lead to large performance improvements. It shows that application-specific protocols substantially improved the performance of three application programs--appbt, em3d, and barnes--over carefully tuned transparent shared memory implementations. The speed-ups were obtained on Blizzard, a fine-grained DSM system running on a 32-node Thinking Machines CM-5.
Major Descriptors: **MEMORY MANAGEMENT** -- PERFORMANCE; *SUPERCOMPUTERS -- **MEMORY MANAGEMENT**
Descriptors: COMPUTER CODES; DATA TRANSMISSION; DISTRIBUTED DATA PROCESSING ; PARALLEL PROCESSING; SYNCHRONIZATION
Broader Terms: COMMUNICATIONS; COMPUTERS; DATA PROCESSING; DIGITAL COMPUTERS; PROCESSING; PROGRAMMING
Subject Categories: 990200* -- Mathematics & Computers
...Author(s): **Hill, M.D** ...

... **Wood, D.A.** (Univ. of Wisconsin, Madison, WI (United States). Computer Sciences Dept.)
Major Descriptors: **MEMORY MANAGEMENT** -- PERFORMANCE...

...SUPERCOMPUTERS -- **MEMORY MANAGEMENT**

4/5,K/24 **(Item 3 from file: 103)**
DIALOG(R)File 103:Energy SciTec

02958383 NOV-90-037043; EDB-90-175627
Title: Cache cconsiderations for multiprocessor programmers
Author(s): **Hill, M.D.** ; Larus, J.R. (Computer Sciences Dept., Univ. of Wisconsin, Madison, WI (US
Source: Communications of the ACM (Association of Computing Machinery) (USA) v 33:8. Coden: CACMA ISSN: 0001-0782
Publication Date: Aug 1990
p 97-102

Contract Number (Non-DOE): MIPS-8957278; CCR-8902536
Document Type: Journal Article
Language: In English
Journal Announcement: EDB9023
Subfile: ETD (Energy Technology Data Exchange). NOV (DOE contractor)
US DOE Project/NonDOE Project: NP
Country of Origin: United States
Country of Publication: United States
Abstract: Although caches in most computers are invisible to programmers, they significantly affect program performance. This is particularly true for cache-coherent, shared-memory multi-processors. This article presents recent research into the performance of parallel programs and its implications for programmers.
Major Descriptors: *ARRAY PROCESSORS -- PARALLEL PROCESSING; *PARALLEL PROCESSING -- COMPUTER CODES
Descriptors: **MEMORY MANAGEMENT** ; PROGRAMMING
Broader Terms: PROGRAMMING
Subject Categories: 990200* -- Mathematics & Computers

Author(s): **Hill, M.D** ...
Descriptors: **MEMORY MANAGEMENT** ;

4/5,K/25 (Item 4 from file: 103)
DIALOG(R)File 103:Energy SciTec

02888382 NOV-90-013067; EDB-90-105624
Title: A VLSI chip set for a multiprocessor workstation Part II: A **memory management** unit and cache controller
Author(s): Jeong, D.K.; **Wood, D.A.** ; Gibson, G.A.; Eggers, S.J.; Hodges, D.A.; Katz, R.H.; Patterson, D.A. (Dept. of Electrical and Computer Sciences, Univ. of California, Berkeley, CA (US
Source: IEEE Journal of Solid-State Circuits (Institute of Electrical and Electronics Engineers) (USA) v 24:6. Coden: IJSCB ISSN: 0018-9200
Publication Date: Dec 1989
p 1699-1707
Contract Number (Non-DOE): 482427-25840
Document Type: Journal Article
Language: In English
Journal Announcement: EDB9014
Subfile: ETD (Energy Technology Data Exchange). NOV (DOE contractor)
US DOE Project/NonDOE Project: NP
Country of Origin: United States
Country of Publication: United States
Abstract: This paper describes a **memory management** unit and a cache controller (MMU/CC) for a shared memory multiprocessor. The MMU/CC implements a novel **memory management** scheme, called in-cache address translation, that does not require a translation lookaside buffer (TLB). It also implements a snooping bus protocol to maintain data consistency across all caches in the system. Both chips are implemented in a 1.6-{mu}m double-layer-metal CMOS technology, and are being used in a multiprocessor workstation (SPUR) successfully executing a UNIX-like network-based operating system called Sprite as well as many applications including LISP programs.
Major Descriptors: *ARRAY PROCESSORS -- INTEGRATED CIRCUITS; *LISP; *MEMORY DEVICES -- DESIGN
Descriptors: PARALLEL PROCESSING
Broader Terms: ELECTRONIC CIRCUITS; MICROELECTRONIC CIRCUITS; PROGRAMMING; PROGRAMMING LANGUAGES
Subject Categories: 990200* -- Mathematics & Computers

Part II: A **memory management** unit and cache controller
...Author(s): **Wood, D.A**
Abstract: This paper describes a **memory management** unit and a cache controller (MMU/CC) for a shared memory multiprocessor. The MMU/CC implements a novel **memory management** scheme, called in-cache

address translation, that does not require a translation lookaside buffer (TLB). It also....

4/5,K/26 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

08988008 PASCAL No.: 90-0156185
A VLSI chip set for a multiprocessor workstation. II: A memory management **unit and cache controller**
DEOG-KYOON JEONG; **WOOD D A** ; GIBSON G A; EGGERS S J; HODGES D A; KATZ R H; PATTERSON D A
Univ. California, dep. electrical eng. & computer sci., Berkeley CA 94720, USA
Journal: IEEE journal of solid-state circuits, 1989, 24 (6) 1699-1707
ISSN: 0018-9200 CODEN: IJSCBC Availability: CNRS-222L
No. of Refs.: 18 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: USA
Language: English
La technologie CMOS a tres grande echelle d'integration permet d'integrer un puissant processeur dans une puce unique. On decrit un circuit realisant la fonction de gestion memoire et de commande de l'antememoire pour un multiprocesseur a memoire partagee

English Descriptors: Multiprocessor; VLSI circuit; Complementary MOS technology; Cache memory; System architecture; Storage management; Workstation
French Descriptors: Multiprocesseur; Circuit VLSI; Technologie MOS complementaire; Antememoire; Architecture systeme; Gestion memoire; Station travail; Architecture RISC

Classification Codes: 250A10G; 001D03J07

A VLSI chip set for a multiprocessor workstation. II: A memory management **unit and cache controller**
DEOG-KYOON JEONG; **WOOD D A** ; GIBSON G A; EGGERS S J; HODGES D A; KATZ R H; PATTERSON D A

4/5,K/27 (Item 1 from file: 239)
DIALOG(R)File 239:Mathsci

01812565 STR 054500
A VLSI chip set for a multiprocessor workstation. Part I: A RISC microprocessor with coprocessor interface and support for symbolic processing. Part II: A memory management **unit and cache controller.**
Eggers, S. J.
Gibson, G. A.
Hill, M. D.
Hodges, D. A.
Jeong, D.-K.
Katz, R. H.
Kong, S. I.
Lee, D. D.
Patterson, D. A.
Taylor, G. S.
Wood, D. A. (University of California, Berkeley, Computer Science Division.
1989,
Language: English
Document Type: Technical Report
Part I by David D. Lee, Shing I. Kong, Mark D. Hill, George S. Taylor, David A. Hodges, Randy H. Katz, and David A. Patterson.; Part II by

Deog-Kyoon Jeong, David A. Wood, Garth A. Gibson, Susan J. Eggers, David A. Hodges, Randy H. Katz, and David A. Patterson.
UCB/CSD 89/500.
Subfile: STR (Stanford Technical Reports)

...**workstation. Part I: A RISC microprocessor with coprocessor interface and support for symbolic processing. Part II: A** memory management **unit and cache controller.**
Eggers, S. J.
Gibson, G. A.
Hill, M. D.
Hodges, D. A.
Jeong, D.-K.
Katz, R. H.
Kong, S. I.
Lee, D. D.
Patterson, D. A.
Taylor, G. S.
Wood, D. A ...

4/5,K/28 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01566211 SUPPLIER NUMBER: 15321120
Cooperative shared memory: software and hardware for scalable multiprocessors. (Technical)
Hill, Mark D. ; Larus, James R.; Reinhardt, Steven K.; **Wood, David A.**
ACM Transactions on Computer Systems, v11, n4, p300(19)
Nov, 1993
DOCUMENT TYPE: Technical ISSN: 0734-2071 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: The small number of massively parallel, shared-memory machines is due to the lack of a shared-memory programming performance model that can determine the cost of operations for programmers and the cases that are common for hardware designers, which lets them build simple hardware to optimize them. The cooperative shared memory approach to shared-memory design is described in an attempt to rectify this situation; the initial implementation uses a simple programming model called Check-In/Check-Out (CICO) along with even simpler hardware called Dir1SW. Programs in CICO bracket uses of shared data with a 'check_out' directive marking the expected first use and a 'check_in' directive terminating the expected use of the data. Communication latency is hidden with the aid of a cooperative prefetch directive. The Dir1SW minimal directory protocol adds little complexity to message-passing hardware but supports programs written within the CICO model efficiently.

SPECIAL FEATURES: illustration; table; chart; graph
DESCRIPTORS: Theoretical Research; Shared Memory; Performance Measurement ; Concurrent Programming; Modeling; **Memory management** ; Multiprocessing; Cache memory
FILE SEGMENT: AI File 88

Hill, Mark D ...

... **Wood, David A.**

...DESCRIPTORS: **Memory management** ;

4/5,K/29 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01478346 SUPPLIER NUMBER: 13885561

Page placement algorithms for large real-indexed caches. (Technical)
Kessler, R.E.; **Hill, Mark D.**
ACM Transactions on Computer Systems, v10, n4, p338(22)
Nov, 1992
DOCUMENT TYPE: Technical ISSN: 0734-2071 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: Both paged virtual memory and caches are supported in most general-purpose computer systems. Most operating systems place pages by selecting an arbitrary page frame from a pool of page frames made available by the page replacement algorithm. A simple model is developed showing that naive, or arbitrary, page placement causes up to 30 percent unnecessary cache conflicts. Several page placement algorithms are presented, called careful-mapping algorithms, that select a page frame from the pool of available page frames that will most likely reduce cache contention. Trace-driven simulation shows that dynamic cache misses can be reduced by between 10 and 20 percent with careful mapping over naive mapping in a direct-mapped real-indexed multimegabyte cache. Careful-mapping algorithms are an inexpensive way to improve cache performance when main memory is underused because it is easy to maintain a large available pool.
SPECIAL FEATURES: illustration; table; chart; graph
DESCRIPTORS: Page Sizing; Research and Development; Algorithm Analysis; New Technique; Cache memory; **Memory management** ; Virtual memory; Operating System
FILE SEGMENT: AI File 88

... **Hill, Mark D.**

...DESCRIPTORS: **Memory management** ;

4/5,K/30 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01477893 SUPPLIER NUMBER: 12907540
Asynchronous transfer mode receiver. (Technical)
Hill, M. ; Cantoni, A.; Moors, T
IEE Proceedings Part E Computers and Digital Techniques, v139, n5, p401(9)
Sept, 1992
DOCUMENT TYPE: Technical ISSN: 0143-7062 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: Asynchronous cell-based transmission is the preferred transmission mode for emerging high-speed network standards such as the IEEE 802.6 metropolitan area network standard and the CCITT broadband integrated services digital network. These networks are envisaged to operate at bit rates in excess of 100 Mbit/s. The high bit rate and the cell-based mode of transmission pose challenging requirements on memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high speed asynchronous-transfer-mode-based network. The paper also discussed a number of major generic issues addressed during the development. (Reprinted by permission of the publisher.)
SPECIAL FEATURES: illustration; chart; table
DESCRIPTORS: **Memory Management** ; Asynchronous; Communications Modes; Packet Switch; Networks
FILE SEGMENT: CD File 275

Hill, M ...

...ABSTRACT: memory-buffer management and the reassembly of packets from constituent cells. The paper describes hardware architecture and **memory - management** techniques developed to achieve the required packet-reassembly functions and buffer- **memory management** for a node operating in a high

speed asynchronous-transfer-mode-based network. The paper also discussed...

DESCRIPTORS: **Memory Management ;**

4/5,K/31 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01388624 SUPPLIER NUMBER: 09379622 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The perfect marriage? (Roderick Manhattan and Associates' Drafix Windows CAD software package) (Software Review) (evaluation)
Wood, David
3D, n28, p29(1)
August, 1990
DOCUMENT TYPE: evaluation ISSN: 0953-2331 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 807 LINE COUNT: 00065

ABSTRACT: Roderick Manhattan and Associates' Drafix Windows CAD is an easy-to-use computer-aided design software package. The package's features include a well-designed users' manual, simple and quick installation procedures, straightforward drawing and editing, and a large selection of line terminators. The disadvantages of the package include a cramped screen and the inability of the Escape key to stop a command. The package requires a 286-, 386-, or 486-based PC with 1Mbyte of RAM. The cost is 695 pounds sterling. The package's capabilities can be improved by the addition of Microsoft Windows 3.0, at a cost of 99 pounds sterling.
CAPTIONS: 3D verdict. (table)
SPECIAL FEATURES: illustration; table
COMPANY NAMES: Roderick Manhattan and Associates--Products
DESCRIPTORS: Graphics Software; Evaluation; Computer-Aided Design
SIC CODES: 7372 Prepackaged software
TRADE NAMES: Drafix Windows CAD (CAD software)--evaluation
OPERATING PLATFORM: Intel 80286; Intel 80386; Intel 80486; MS Windows
FILE SEGMENT: CD File 275

Wood, David
... the ultimate success of the package will depend on the performance of the new environment. its' improved **memory management** , however, means extended memory above 1Mbyte, and so faster file loading, zooms and redraws.
In general Drafix...

4/5,K/32 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01380483 SUPPLIER NUMBER: 09605981 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Port Windows applications to OS/2 (almost) painlessly with the Software Migration Kit.
Fogelin, Eric; **Wood, David** ; Bergman, Noel
Microsoft Systems Journal, v5, n6, p21(10)
Nov, 1990
ISSN: 0889-9932 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4150 LINE COUNT: 00332

ABSTRACT: Microsoft Corp's Microsoft Windows to OS/2 Software Migration Kit (SMK) is a set of software tools that makes porting applications from the Microsoft Windows graphical environment to OS/2 Presentation Manager (PM) much easier. SMK acts as an extension to the Microsoft Windows Software Development Kit Version 3.0 (SDK). SMK reduces conversion time for large applications from months to days with its mapping layer that translates Windows function calls into OS/2 function calls. The code layer is implemented as a set of OS/2 dynamic-link libraries (DLLs). It sits between PM and the Windows application and translates calls to the Windows

application program interface (API) at run time. The mapping layer accepts the Windows API call, interprets it and reorders and converts the parameters. It then calls the corresponding PM API. Details on using the SMK are presented.
CAPTIONS: Software Migration Kit mapping layer. (chart); Beta SMK contents. (chart); Windows functions unsupported in SMK. (chart)

SPECIAL FEATURES: illustration; chart
COMPANY NAMES: Microsoft Corp.--Products
DESCRIPTORS: Software Migration; Application Development Software; Coding ; GUI
TICKER SYMBOLS: MSFT
TRADE NAMES: Microsoft Windows (GUI)--Programming; Microsoft Windows to OS/2 Software Migration Kit (Program development software)--Usage
OPERATING PLATFORM: OS/2 PM; MS Windows
FILE SEGMENT: CD File 275

... **Wood, David**
... Windows API functions are supported in the SMK mapping layer, with the execution of sound, 32-bit **memory management** , some Graphic Device Interface (GDI) functions, and a few other functions (see Figure 8). These functions must...

4/5,K/33 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01273978 SUPPLIER NUMBER: 08090746
Evaluating associativity in CPU caches. (technical)
Hill, Mark D. ; Smith, Alan Jay
IEEE Transactions on Computers, v38, n12, p1612(19)
Dec, 1989
DOCUMENT TYPE: technical ISSN: 0018-9340 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: Cache memories are generally designed to be direct-mapped or set-associative as large fully-associative caches are usually infeasible and/or too expensive. Efficient new algorithms for the simulation of alternative direct-mapped and set-associative caches are presented, and the uses of those algorithms to quantify the effect of limited associativity on the cache miss ratio are described. Three important cache parameters are cache size, block/line size and associativity, the last being emphasized here.
CAPTIONS: Set-associative mapping. (chart); Data on traces. (table); Miss ratios for five-trace workload with caches of four associativities. (graph)

SPECIAL FEATURES: illustration; chart; table; graph
DESCRIPTORS: Cache Memory; Algorithm Analysis; Processor Architecture; Associative Memory; Simulation of Computer Systems; CPU; **Memory Management** ; Research and Development; Memory Mapping; New Technique
FILE SEGMENT: AI File 88

Hill, Mark D ...

...DESCRIPTORS: **Memory Management** ;

4/5,K/34 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2004 CMP Media, LLC. All rts. reserv.

01116582 CMP ACCESSION NUMBER: EET19970120S0074
Euphony: a signal processor for ATM
Peter Z. Onufryk, Principal Technical Staff Member, Consumer Electronics, Research Department, AT&T Labs, Murray Hill, N.J.
ELECTRONIC ENGINEERING TIMES, 1997, n 937, PG54

```
Set     Items   Description
S1      72823   (TRANSLATION OR TABLE)()(LOOKASIDE OR LOOK()ASIDE)()BUFFER?
             OR TLB OR MAP OR MAPPING OR MAPS OR MAPPED
S2    1003101   CONTEXT OR CURRENT()STATUS OR CONDITION OR MODE
S3     369497   VALID? OR AUTHENTICAT? OR VERIF? OR CERTIF? OR IDENTIF?
S4    1772779   MEMORY OR STORAGE OR CACHE? OR BUFFER?
S5       1444   S1 AND S2 AND S3
S6      17502   S2 (3N) S4
S7        279   S1 AND S6
S8       2168   S3 (2N)(FLAG? OR INDICATOR? OR POINTER?)
S9          3   S7 AND S8
S10        26   S7 AND S3
S11        26   S9 OR S10
S12        17   S11 AND IC=G06F?
S13         2   S5 AND (DEMAPPING OR DEMAP OR DEMAPS OR DEMAPPED)
S14         1   S13 NOT S11
S15        27   S11 OR S14
S16         3   S15 AND MC=(T01-F05E? OR T01-H01B3 OR T01-S03)
S17        18   S12 OR S14 OR S16
File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200419
         (c) 2004  Thomson Derwent
```

17/5/1 **(Item 1 from file: 347)**
DIALOG(R)File 347:JAPIO

06947911 **Image available**
COMPUTER SYSTEM

PUB. NO.: 2001-175463 [JP 2001175463 A]
PUBLISHED: June 29, 2001 (20010629)
INVENTOR(s): YAGI TATSUO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 11-357769 [JP 99357769]
FILED: December 16, 1999 (19991216)
INTL CLASS: **G06F-009/06** ; **G06F-009/445** ; **G06F-012/06**

ABSTRACT

PROBLEM TO BE SOLVED: To provide a computer system for providing a boot program area, without suppressing program area by using a relatively smaller-scaled microcomputer, and **validly** utilizing a memory space.

SOLUTION: This computer system is provided with a control means 1 for executing an instruction according to program data, a rewritable first memory means 8 for storing a boot program, a rewritable second memory means 9 for storing an operation program, a mode switching means 7 for selecting either a boot mode or an operation **mode** , and a **memory map** converting means 5 for switching the address of the first and second memory means according to the mode selected by the **mode** switching means. The **memory map** converting means sets the address of the first and second memory means, so that the operation program can be written in the second memory means according to the boot program in the boot mode, and sets the address of the first and second memory means, so that a prescribed instruction can be executed by a control means according to the operation program in the operation mode.

17/5/2 **(Item 2 from file: 347)**
DIALOG(R)File 347:JAPIO

06608713 **Image available**
DEVICE, SYSTEM, AND METHOD FOR PRINT PROCESSING AND COMPUTER-READABLE RECORDING MEDIUM WHERE PROGRAM ALLOWING COMPUTER TO IMPLEMENT SAME METHOD IS RECORDED

PUB. NO.: 2000-194518 [JP 2000194518 A]
PUBLISHED: July 14, 2000 (20000714)
INVENTOR(s): NISHINOSONO MICHIAKI
APPLICANT(s): RICOH CO LTD
APPL. NO.: 10-376251 [JP 98376251]
FILED: December 24, 1998 (19981224)
INTL CLASS: **G06F-003/12** ; B41J-029/46

ABSTRACT

PROBLEM TO BE SOLVED: To efficiently print only an altered page, to reduce a waste of printing papers, and to save resources by comparing new print data with print data corresponding to **identification** information included in a print request stored in a storage means, page by page, and printing only the page wherein the new print data is detected.

SOLUTION: A control part 127 performs a normal print process when mode data received from a computer 110 together with print data indicates 'normal print mode' and performs the normal print processing and also stores data expanded into a bit **map** in a print data storage part 124 when it is a ' **storage** print **mode** '. When the data indicates a 'difference print mode', only print data (bit **map** data) of a page having different contents

detected by a comparing process part 125 is outputted to a print part 126 and the print data stored in the print data storage part 124 are updated with the print data of the page having the different contents.

17/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02966251 **Image available**
ADDRESS CONVERTER

PUB. NO.: 01-263851 [JP 1263851 A]
PUBLISHED: October 20, 1989 (19891020)
INVENTOR(s): TAKAGI KATSUAKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-091550 [JP 8891550]
FILED: April 15, 1988 (19880415)
INTL CLASS: [4] **G06F-012/10 ; G06F-012/12**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 42.4 (ELECTRONICS -- Basic Circuits)
JOURNAL: Section: P, Section No. 990, Vol. 14, No. 21, Pg. 122, January 17, 1990 (19900117)

ABSTRACT

PURPOSE: To simplify the constitution of a circuit which is used for control of the replacement of entries by adding a using condition bit control circuit to the outside of a memory array to prepare a using **condition** bit within the **memory** array and to apparently turn forward or reverse the using condition bit.

CONSTITUTION: An address converting device (**TLB**) 1 contains a mask circuit 11, an associative array 12, a coincident line processing circuit 13, and a data array 14. The array 12 includes an LA field 123 which holds a **valid** bit 122, a using condition bit 121 and a part (to undergo the address conversion) of a logical address. A mask pattern is produced by a mask pattern generating circuit 15 under the control of a control signal 34. A using condition bit control circuit consisting of a flip-flop 21 and an EOR gate 22 turns apparently forward or reverse the contents of the bit 121.

17/5/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015430491 **Image available**
WPI Acc No: 2003-492633/200346
XRPX Acc No: N03-391327
Virtual memory control method in computer system, involves setting translation entry mapping **indicator for each entry associated with given** context **of** memory **and demapping given** context **by changing set** mapping **indicator**
Patent Assignee: CASSIDAY D R (CASS-I); FEEHRER J R (FEEH-I); HILL M D (HILL-I); JACKSON C J (JACK-I); OSTROVSKY B (OSTR-I); PILLAI P (PILL-I); WOOD D A (WOOD-I)
Inventor: CASSIDAY D R; FEEHRER J R; HILL M D; JACKSON C J; OSTROVSKY B; PILLAI P; WOOD D A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030070058	A1	20030410	US 2001973279	A	20011009	200346	B

Priority Applications (No Type Date): US 2001973279 A 20011009

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030070058 A1 10 G06F-012/10

Abstract (Basic): US 20030070058 A1
NOVELTY - A translation entry **mapping** indicator (132) is set for each entry associated with the given **context** (134) of **memory** and a **validity flag** (130) is set for each entry associated with the given context. The given context is demapped by changing the **mapping** indicator set for each given context.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory management device; and program for controlling virtual memory in computer system.
USE - For controlling physical memory of computer system.
ADVANTAGE - The time required to demap the given context is reduced without degrading the performance of the computer system. Thereby the memory management process is performed efficiently.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of memory management unit.
context **mapping** indicator (122)
clean-up indicator (124)
validity flag (130)
translation entry **mapping** indicator (132)
context (134)
pp; 10 DwgNo 2/5
Title Terms: VIRTUAL; MEMORY; CONTROL; METHOD; COMPUTER; SYSTEM; SET; TRANSLATION; ENTER; **MAP** ; INDICATE; ENTER; ASSOCIATE; CONTEXT; MEMORY; CONTEXT; CHANGE; SET; **MAP** ; INDICATE
Derwent Class: T01
International Patent Class (Main): **G06F-012/10**
File Segment: EPI

17/5/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014979469 **Image available**
WPI Acc No: 2003-039984/200303
XRPX Acc No: N03-031338
Real-time access providing apparatus for flash memory device in cellular phone, includes control logic which accesses flash memory **data, when flash** condition **is encountered**
Patent Assignee: GARNER R P (GARN-I); INTEL CORP (ITLC)
Inventor: GARNER R P; GARNER R
Number of Countries: 100 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020136078	A1	20020926	US 2001815767	A	20010323	200303	B
WO 200295592	A2	20021128	WO 2002US22516	A	20020214	200304	
US 6549482	B2	20030415	US 2001815767	A	20010323	200329	

Priority Applications (No Type Date): US 2001815767 A 20010323
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020136078 A1 14 G11C-008/00
WO 200295592 A2 E G06F-012/00
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
US 6549482 B2 G11C-008/00

Abstract (Basic): US 20020136078 A1

NOVELTY - A memory **mapped** input/output unit (12) is used to access flash memory data, when a particular condition is encountered. The condition is not a flash read command instruction. A control logic accesses the flash memory data, when the flash condition is encountered.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Flash memory device; and

(2) Real-time access provision method.

USE - For providing real-time access to flash memory device such as electrically erasable programmable read only memory used in cellular phone.

ADVANTAGE - As the need to switch between modes to access flash data while performing another function is eliminated, the performance and speed are improved. As the memory **mapped** input/output registers hold various parameters needed to **identify** features of the flash device, the real-time access to flash memory is provided efficiently.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of logical **mapping** of flash configuration plane to memory **mapped** input/output portion.

Input/output unit (12)

pp; 14 DwgNo 1/6

Title Terms: REAL; TIME; ACCESS; APPARATUS; FLASH; MEMORY; DEVICE; CELLULAR ; TELEPHONE; CONTROL; LOGIC; ACCESS; FLASH; MEMORY; DATA; FLASH; CONDITION; ENCOUNTER

Derwent Class: T01; U14; U21; W01

International Patent Class (Main): **G06F-012/00** ; G11C-008/00

File Segment: EPI

17/5/6 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014698192 **Image available**

WPI Acc No: 2002-518896/200255

XRPX Acc No: N02-410777

Transmission apparatus e.g. ATM apparatus in communication network, maps identified **extended cell which is output from controller onto payload of another frame signal for transmission**

Patent Assignee: FUJITSU LTD (FUIT); KAWANO J (KAWA-I); NATANI M (NATA-I) ; SUZUKI A (SUZU-I); SUZUKI Y (SUZU-I)

Inventor: KAWANO J; NATANI M; SUZUKI A; SUZUKI Y

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020065073	A1	20020530	US 2001901198	A	20010709	200255	B
JP 2002171258	A	20020614	JP 2000364098	A	20001130	200255	

Priority Applications (No Type Date): JP 2000364098 A 20001130

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020065073	A1		52	H04Q-007/20	
JP 2002171258	A		30	H04L-012/28	

Abstract (Basic): US 20020065073 A1

NOVELTY - The multiplexing and **demapping** unit demultiplexes and **demaps** the extended ATM cells from a payload of frame signal received from a transmission path. A cell synchronizer executes a cell synchronization processing to **identify** an extended cell boundary. The multiplexing and **mapping** unit multiplexes and **maps** an extended cell which is output from a controller onto a payload of another frame signal for transmission to the transmission path.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Communication network;

(2) SDH transmission apparatus;

(3) Extended cell communication network; and

(4) Add/drop multiplexing apparatus.

USE - E.g. asynchronous transfer **mode** (ATM) transmission apparatus, synchronous digital hierarchy (SDH) transmission apparatus (claimed), add/drop multiplexer (claimed), ADM transmission apparatus in communication network (claimed) with extended cell communication network, ATM cell transmission network, SONET/SDH network, local area network (LAN), wide area network (WAN), IP network, photonic network e.g. OADM, WDM network.

ADVANTAGE - Extended ATM cell apparatus can be transmitted at high speed through an SDH transmission apparatus and makes it possible to enhance the performance of an SDH transmission apparatus. The route status of a bypass virtual path can be monitored at all times, thereby making it possible to provide for change out of a virtual path, when a failure occurs.

DESCRIPTION OF DRAWING(S) - The figure shows the extended cell communication network.

pp; 52 DwgNo 1/40

Title Terms: TRANSMISSION; APPARATUS; ATM; APPARATUS; COMMUNICATE; NETWORK; **MAP** ; **IDENTIFY** ; EXTEND; CELL; OUTPUT; CONTROL; PAYLOAD; FRAME; SIGNAL; TRANSMISSION

Derwent Class: T01; W01

International Patent Class (Main): H04L-012/28; H04Q-007/20

International Patent Class (Additional): H04J-003/00; H04J-003/14; H04L-001/22; H04L-012/437

File Segment: EPI

17/5/7 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014295907 **Image available**

WPI Acc No: 2002-116610/200216

XRPX Acc No: N02-087092

File recording method involves forming cluster by recording file of arbitrary recording length at arbitrary positions of memory section and recording data recording positional information and protection information

Patent Assignee: SONY CORP (SONY)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001043112	A	20010216	JP 99217133	A	19990730	200216	B

Priority Applications (No Type Date): JP 99217133 A 19990730

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001043112	A		151	G06F-012/00	

Abstract (Basic): JP 2001043112 A

NOVELTY - Cluster (UC1) is formed by recording file of arbitrary recording length (Ln1) at arbitrary positions (ad10) of the memory section (Mem1). Data recording positional information (CAdT) showing the recording position of the cluster is recorded at a fixed position (adC) and protection information (Pdv,Pdw) for every cluster is recorded at arbitrary positions (adPLS).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) File reproduction method;

(b) Data write-in system;

(c) Data reading system;

(d) Data recording and reproducing apparatus;

(e) Data write-in apparatus;

(f) Data reader;

(g) Recording medium

USE - For data recording and reproducing apparatus.

ADVANTAGE - Improves memory utilization efficiency by preventing

the generation of unused recording area and simplifies file control operation. Reduces the area required for recording protection information. Enables to access the desired cluster reliably.

Identifies recording position easily and protects file reliably. Enables to confirm recording **condition** on the **memory** . Simplifies acquisition of protection information and improves compatibility with memories having different recording capacities. Improves data recording and regeneration efficiency and enables to confirm write-in approval at arbitrary positions on the recording medium easily.

DESCRIPTION OF DRAWING(S) - The figure shows the explanatory drawing of the memory **map** of the memory section in which data is recorded by a data write-in system. (Drawing includes non-English language text).

Recording positions (adc,adPLS)
Positional information (CAdT)
Protection information (Pdv,Pdw)
Memory section (Ln1)
Memory section (Mem1)
Cluster (UC1)
pp; 151 DwgNo 4/43

Title Terms: FILE; RECORD; METHOD; FORMING; CLUSTER; RECORD; FILE; ARBITRARY; RECORD; LENGTH; ARBITRARY; POSITION; MEMORY; SECTION; RECORD; DATA; RECORD; POSITION; INFORMATION; PROTECT; INFORMATION
Derwent Class: T01; T03
International Patent Class (Main): **G06F-012/00**
International Patent Class (Additional): **G06F-012/02** ; **G06F-012/14** ; G06K-019/073; G11B-020/10
File Segment: EPI

17/5/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013851854 **Image available**
WPI Acc No: 2001-336067/200136
Related WPI Acc No: 2001-336048
XRPX Acc No: N01-242587

Vault controller for secure multiple browser session in e-commerce uses context manager to activate keys for transferring data in storage levels and initiate application interface within domain/function as defined by URL

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CARROLL R B; FISK M D; GHAFIR H; MARUYAMA H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CA 2310535	A1	20001230	CA 2310535	A	20000602	200136	B

Priority Applications (No Type Date): US 99343231 A 19990630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CA 2310535	A1	E	24	G06F-017/30	

Abstract (Basic): CA 2310535 A1

NOVELTY - A registration authority (20) reviews submitted requests and the decision is provided to a **certification** agent (29). The vault controller uses browser client **authentication** and SSL protocol with browser request encrypted and sent to the vault controller software along with an access **certificate** . The vault supervisor **validates** and **maps** access **certificate** to a user ID and password.

DETAILED DESCRIPTION - Embedded in the vault process is a context manager that includes data structure for storing global context made up of variables and their values, in memory as well as mechanism for importing and exporting global **context** to external encrypted **storage** . An external vault agent (28) running remotely incorporates a subset of vault process functionality, enabling agent to exchange secure

messages with vault running under the vault controller. The vault process is multithreaded with each thread with its own local storage area allowing it to maintain 'state' across multiple browser-server interactions. An INDEPENDENT CLAIM is also included for a context manager within a vault process for maintaining state information between successive user browser sessions.

USE - For secure browsing in e-commerce.

ADVANTAGE - It supports the creation, storage and retrieval of data for state maintenance of vault processes in successive browser connection as well as across multiple units/work and/or separate applications.

DESCRIPTION OF DRAWING(S) - The figure shows a representation of a vault controller in a secure end-to-end communication system interacting with users, vault agents and registration authorities.

pp; 24 DwgNo 1/4

Title Terms: VAULT; CONTROL; SECURE; MULTIPLE; SESSION; CONTEXT; MANAGE; ACTIVATE; KEY; TRANSFER; DATA; STORAGE; LEVEL; INITIATE; APPLY; INTERFACE ; DOMAIN; FUNCTION; DEFINE

Derwent Class: W01

International Patent Class (Main): **G06F-017/30**

International Patent Class (Additional): **G06F-017/60** ; H04L-012/16

File Segment: EPI

17/5/9 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011482112 **Image available**

WPI Acc No: 1997-460017/199743

XRPX Acc No: N97-383008

Address translation control for processor and translation look aside buffer **- has circuitry coupled to storage elements outputting translation Hit signal indicating that** translation look aside buffer **is currently storing physical address when context** identification **number equals selected context number**

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: MOHAMED A H

Number of Countries: 008 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 797149	A2	19970924	EP 97301874	A	19970320	199743	B
JP 10083352	A	19980331	JP 9787210	A	19970324	199823	
US 5754818	A	19980519	US 96620464	A	19960322	199827	
EP 797149	B1	20011010	EP 97301874	A	19970320	200167	
DE 69707181	E	20011115	DE 607181	A	19970320	200176	
			EP 97301874	A	19970320		

Priority Applications (No Type Date): US 96620464 A 19960322

Cited Patents: No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 797149	A2	E	15	G06F-012/10	
Designated States (Regional): DE FR GB IT NL SE					
JP 10083352	A		15	G06F-012/10	
US 5754818	A			G06F-012/10	
EP 797149	B1	E		G06F-012/10	
Designated States (Regional): DE FR GB IT NL SE					
DE 69707181	E			G06F-012/10	Based on patent EP 797149

Abstract (Basic): EP 797149 A

The address translation control circuit includes several **context storage** elements. The first one contains a first context number, and a second one a second context number. Circuitry is coupled to the storage elements which outputs a translation Hit signal.

The Hit signal indicates that the **translation look aside buffer** (308) is currently storing the physical address when the

context **identification** number equals a selected context number. The equalled selected context number is either the first or the second context number and the pre-stored virtual address is equivalent to the requested virtual address.

ADVANTAGE - Improves performance of electronic addressing by sharing translation table entries of **translation look aside buffer** .

Dwg.3/6

Title Terms: ADDRESS; TRANSLATION; CONTROL; PROCESSOR; TRANSLATION; ASIDE; BUFFER; CIRCUIT; COUPLE; STORAGE; ELEMENT; OUTPUT; TRANSLATION; HIT; SIGNAL; INDICATE; TRANSLATION; ASIDE; BUFFER; CURRENT; STORAGE; PHYSICAL; ADDRESS; CONTEXT; **IDENTIFY** ; NUMBER; EQUAL; SELECT; CONTEXT; NUMBER

Derwent Class: T01

International Patent Class (Main): **G06F-012/10**

File Segment: EPI

17/5/10 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011073604 **Image available**

WPI Acc No: 1997-051528/199705

XRPX Acc No: N97-042420

Memory data access system for computer system using virtual memory addressing - uses virtual tags for identifying **page table** pointers **at predetermined level of table higher than initial context level and stores tags in tag memory of** translation look aside buffer

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: LOPEZ-AGUADO H; MEHRING P A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5586283	A	19961217	US 93132796	A	19931007	199705	B

Priority Applications (No Type Date): US 93132796 A 19931007

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5586283	A		14	G06F-012/10	

Abstract (Basic): US 5586283 A

In a computer system comprising a processor and memory, accesses to memory are performed by issuing a virtual address to memory. An appts. for performing a translation from a virtual address to a physical address has a **translation look aside buffer** comprising a page table memory comprising a number of levels of a page table, an initial level of the page table being **identified** as a root level, the page table memory storing page table pointers (PTPs) which provide a base address of a table in a next higher level of a page table and page table entries (PTEs) which provide information to translate the virtual address to the physical address. A tag memory comprises tags, which comprise **identification** of PTEs and PTPs. The tags also comprise virtual PTP tags for PTPs located in at least one predetermined higher level that is higher than the root level, and provide a pointer to a corresponding entry in the page table.

A select mechanism is coupled to receive the virtual address and **context** of the **memory** access, and generates a compare virtual PTP tag if a **TLB** miss occurs when trying to access a tag **identifying** a PTE corresponding to the virtual address. The compare virtual PTP tag is generated from the **context** of the **memory** address and a predetermined portion of the virtual address. The compare virtual PTP tag is compared to stored virtual PTP tags stored in the tag memory such that if the compared virtual PTP tag and one of the stored virtual PTP tags match, the select mechanism provides a pointer to the corresp. PTP at the predetermined higher level of the page table without performing a page table walk initiating at the root level through the lower level page tables.

ADVANTAGE - Time expended for performing a page table walk is minimized. Decreases latencies caused by accesses to increasing levels of page tables during table walk of page table, by eliminating time required to walk through root and first levels of page table.

Dwg.9/9

Title Terms: MEMORY; DATA; ACCESS; SYSTEM; COMPUTER; SYSTEM; VIRTUAL; MEMORY; ADDRESS; VIRTUAL; TAG; **IDENTIFY** ; PAGE; TABLE; POINT; PREDETERMINED; LEVEL; TABLE; HIGH; INITIAL; CONTEXT; LEVEL; STORAGE; TAG; TAG; MEMORY; TRANSLATION; ASIDE; BUFFER

Derwent Class: T01

International Patent Class (Main): **G06F-012/10**

File Segment: EPI

17/5/11 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011021298 **Image available**

WPI Acc No: 1996-518248/199651

XRPX Acc No: N96-436762

Access control appts for access register translation lookaside buffer , **in computer system - generates and stores ALB** identifier **(ALBID) in host ALBID register and marks** valid **ALBID** validity indicator **in host ALBID register when host mode is initiated on logical processor**

Patent Assignee: AMDAHL CORP (AMDA)

Inventor: CONNELL J J; LIPMAN P H; RYBA E G; WEISS D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5574936	A	19961112	US 92816864	A	19920102	199651	B
			US 94257457	A	19940609		
			US 95378082	A	19950125		

Priority Applications (No Type Date): US 92816864 A 19920102; US 94257457 A 19940609; US 95378082 A 19950125

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5574936	A		30	G06F-012/00	Cont of application US 92816864
					Cont of application US 94257457

Abstract (Basic): US 5574936 A

The appts includes a host ALBID register for storing an ART-lookaside buffer (ALB) **identifier** (ALBID) and an ALBID **validity indicator** for the host mode of a logical processor. A guest ALBID register for storing an ALB **identifier** and an ALB ID **validity indicator** for the most recent guest mode on the logical processor. An ALB **identifier** (ALBID) is generated and stored in the host ALBID register and marks **valid** the ALBID **validity indicator** in the host ALBID register when a host mode is initiated on the logical processor. An ALB **identifier** (ALBID) is generated and stored in the guest ALBID register and marks **valid** the ALBID **validity indicator** in the guest ALBID register when a guest mode is first initiated on the logical processor.

ADVANTAGE - Preserves logical integrity of access register **translation** lookaside **buffer** across **context** switches.

Dwg.1/11

Title Terms: ACCESS; CONTROL; APPARATUS; ACCESS; REGISTER; TRANSLATION; BUFFER; COMPUTER; SYSTEM; GENERATE; STORAGE; **IDENTIFY** ; HOST; REGISTER; MARK; **VALID** ; **VALID** ; INDICATE; HOST; REGISTER; HOST; MODE; INITIATE; LOGIC; PROCESSOR

Derwent Class: T01

International Patent Class (Main): **G06F-012/00**

File Segment: EPI

Inventor: CHENG R; GARNER R; JOY W; MORAN J; SHANNON W; VAN LOO W; WATKINS J; VANLOO W; LOO W V
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3832912	A	19890503	DE 3832912	A	19880928	198921	B
AU 8822424	A	19890406				198921	
FR 2621407	A	19890407				198921	
GB 2210480	A	19890607	GB 8819018	A	19880810	198923	
GB 2210480	B	19920129				199205	
CA 1305800	C	19920728	CA 577050	A	19880909	199236	
DE 3832912	C2	19981203	DE 3832912	A	19880928	199901	
US 5845325	A	19981201	US 87104280	A	19871002	199904	
			US 90603248	A	19901024		
			US 9346476	A	19930413		

Priority Applications (No Type Date): US 87104280 A 19871002; US 90603248 A 19901024; US 9346476 A 19930413
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3832912	A		34		
US 5845325	A			G06F-015/16	Cont of application US 87104280
					Cont of application US 90603248
CA 1305800	C			G06F-012/08	
DE 3832912	C2			G06F-012/08	

Abstract (Basic): DE 3832912 A

The intelligent work station contains a CPU e.g. MC68020, a direct-**mapped** block-organised cache memory, a buffer memory for writing back the cache, a tag memory (virtual address and status bits for each cache block), a memory management unit (MMU) to assign and reclaim memory workspace, a main memory, cache 'hit' detector logic, cache memory flush logic and work station control logic. Also optionally, a context ident (ID) register to **identify** and prioritise active processes in multi-tasking, cache flush logic to enhance flushing performance, direct virtual memory access (DVMA) logic, a multiplexer and a databuss buffer to extend from 32 to 64 data bits.

Addressing is extended to contain bits defining segment, page and block number as well as physical address, with optional context ID bits. The operating system kernel of, e.g. UNIX (RTM), is expanded to provide a set of commands to flush specific context, segment and page areas of the cache, i.e. spool contents to main memory and release cache space for reassignment. Each cache block has status bits in its tag to define write-back data **valid** and/or modified, two security bits, a supervisor's security bit and a Write Permit bit. Cache 'hit' occurs when content is **valid** , CPU virtual address agrees with that in tag **memory** and, optionally, when **context** ID's agree.

USE/ADVANTAGE - High performance 32 bit multi-user systems. Fast processing in cache memory proceeds transparently to user

Title Terms: WORK; STATION; MULTI; USER; COMPUTER; SYSTEM; VIRTUAL; ADDRESS; CACHE; MEMORY
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-015/16**
International Patent Class (Additional): **G06F-012/10**
File Segment: EPI

17/5/15 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007625004 **Image available**
WPI Acc No: 1988-258936/198837
XRPX Acc No: N88-196545
Concurrent context memory **management unit - uses multiple and concurrent** mapping **tables** identified **by transmission of bits with each data transfer operation**

Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T BELL LAB (AMTT)
Inventor: JENSEN C W; KELLER F R
Number of Countries: 005 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 282213	A	19880914	EP 88301751	A	19880301	198837	B
US 5293597	A	19940308	US 8723858	A	19870309	199410	
			US 90529765	A	19900525		
			US 91737961	A	19910730		

Priority Applications (No Type Date): US 8723858 A 19870309; US 90529765 A 19900525; US 91737961 A 19910730
Cited Patents: 1.Jnl.Ref; A3...9117; No-SR.Pub; US 4145738; US 4355355
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 282213	A	E	8		
Designated States (Regional): DE FR GB IT					
US 5293597	A		7	G06F-012/10	Cont of application US 8723858
					Cont of application US 90529765

Abstract (Basic): EP 282213 A

The memory management unit (10) with its **cache memory** (102) and **mode** control (106) stores and retrieves information from a memory (12) using virtual address tables (404). It performs translations between virtual addresses received in response to instructions from sources having the same virtual address **mapped** to different physical addresses.

The tables (404) contain translation information for each **mapped** pair of virtual and physical addresses. The pair to be utilised in translation is selected by the appropriate process (103,104 or 105) in accordance with the mode information associated (106) with each virtual address.

USE/ADVANTAGE - In multiple concurrent processing. Interprocess data transfer is facilitated with no need to construct temporary **mapping** tables or to switch memory management unit back and forth among processes in course of execution, readout and writing.

1/5

Title Terms: CONCURRENT; CONTEXT; MEMORY; MANAGEMENT; UNIT; MULTIPLE; CONCURRENT; **MAP** ; TABLE; **IDENTIFY** ; TRANSMISSION; BIT; DATA; TRANSFER; OPERATE
Derwent Class: T01
International Patent Class (Main): **G06F-012/10**
International Patent Class (Additional): **G06F-009/46** ; **G06F-012/14**
File Segment: EPI

17/5/16 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004701137
WPI Acc No: 1986-204479/198631
XRPX Acc No: N86-152765

High lighting and classifying segments on CRT display - having segments located in memory **to satisfy matching** condition **so operator can direct terminal to blink**

Patent Assignee: TEKTRONIX INC (TEKT)
Inventor: DALRYMPLE J C; MAYNARD J H; PAUL B G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4601021	A	19860715	US 84684962	A	19841219	198631	B

Priority Applications (No Type Date): US 82367525 A 19820412; US 84684962 A 19841219
Patent Details:

```
Set     Items   Description
S1       5446   (TRANSLATION OR TABLE)()(LOOKASIDE OR LOOK()ASIDE)()BUFFER?
              OR TLB OR MAP OR MAPPING OR MAPS OR MAPPED
S2       3498   CONTEXT OR CURRENT()STATUS OR CONDITION OR MODE
S3       9451   VALID? OR AUTHENTICAT? OR VERIF? OR CERTIF? OR IDENTIF?
S4       8686   MEMORY OR STORAGE OR CACHE? OR BUFFER?
S5         28   S1 AND S2 AND S3
S6          3   S5 AND S4
S7          2   S6 NOT PY>2001
S8          2   S7 NOT PD>20011009
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/Feb
         (c)2004 Info.Sources Inc
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8/5/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01712116 DOCUMENT TYPE: Product

PRODUCT NAME: Virtual-CPU (712116)

Summit Design Inc (574511)
35 Corporate Dr
Burlington, MA 01803 United States
TELEPHONE: (781) 685-4954

RECORD TYPE: Directory

CONTACT: Sales Department

Summit Design's Virtual-CPU is a co- **verification** environment that allows embedded systems developers to analyze and **validate** interactions between hardware and software. Developers can employ Virtual-CPU for system architecture **validations** before hardware implementations are complete. The product can be configured for any standard or customized processor or bus. Virtual-CPU's execution environment runs embedded system software as if it were running on target CPUs. These simulations are linked to logic simulations of embedded system hardware. Virtual-CPU can run in host-code execution **mode** on workstations or in target-code execution **mode** within an Instruction Set Simulator (ISS). Embedded system hardware is modeled in C, C++, or in a hardware description language. Embedded system software is written in C, C++, or in a target processor's assembly language. Employing Virtual-CPU, developers can use existing debugging tools. A **memory map** feature allows designers to swap models.

DESCRIPTORS: CAD; CAD CAM; CAE; Computer Equipment; Coverification; Cross Development; Electrical Engineering; Embedded Systems; Program Development; Simulation

HARDWARE: HP; IBM PC & Compatibles; Sun; UNIX
OPERATING SYSTEM: HP-UX; Linux; Solaris; Windows NT/2000
PROGRAM LANGUAGES: C; C++; Verilog
TYPE OF PRODUCT: Mini; Micro; Workstation
POTENTIAL USERS: Embedded System Design, Coverification
PRICE: Available upon request

REVISION DATE: 20020930

8/5/2
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00080724 DOCUMENT TYPE: Review

PRODUCT NAMES: Windows Application Binary Interface (Wabi) 2.0 (454681)

TITLE: A Less Wobbly Wabi
AUTHOR: Tamasanis, Doug
SOURCE: Byte, v20 n7 p159(2) Jul 1995
ISSN: 0360-5280
HOMEPAGE: http://www.byte.com

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: B

Sun Microsystems' Wabi 2.0 (Windows Application Binary Interface) is used for running Windows applications on UNIX. The earlier version's performance was poor and application support limited. Version 2.0 is now more powerful

and faster, and supports OLE 2.0. It can run in 386 enhanced **mode** , and uses less **memory** . However, it still lacks sound support and support for the Win32 APIs. The lack of application support has been overcome by encouraging users to install Windows 3.1, which is now **certified** to run with Wabi 2.0. There are 24 **certified** applications, which Sun indicates make up over 80 percent of the commercial Windows market. Instead of using emulation, Wabi uses API translation. Translation makes use of the X GUI, by **mapping** Windows commands to X commands. Each user must load a copy of Windows, which on a multi-user system can consume a substantial amount of **memory** . Performance is better than the earlier release, although still somewhat slow.

PRICE: $225

COMPANY NAME: Sun Microsystems Inc (385557)
SPECIAL FEATURE: Screen Layouts
DESCRIPTORS: IBM PC & Compatibles; Integration Software; Interfaces; Program Development; Sun; UNIX; Windows; X Window
REVISION DATE: 19990830

```
Set     Items   Description
S1     456903   (TRANSLATION OR TABLE)()(LOOKASIDE OR LOOK()ASIDE)()BUFFER?
              OR TLB OR MAP OR MAPPING OR MAPS OR MAPPED
S2    1477228   CONTEXT OR CURRENT()STATUS OR CONDITION OR MODE
S3    1749035   VALID? OR AUTHENTICAT? OR VERIF? OR CERTIF? OR IDENTIF?
S4     912475   MEMORY OR STORAGE OR CACHE?.OR BUFFER?
S5       5015   S1 AND S2 AND S3
S6       5311   S2 (3N) S4
S7        159   S1 AND S6
S8       1629   S3 (2N)(FLAG? OR INDICATOR? OR POINTER?)
S9          0   S7 AND S8
S10        18   S7 AND S3
S11       213   S5 AND S4
S12         0   S11 AND S8
S13         0   S5 AND (DEMAPPING OR DEMAP OR DEMAPS OR DEMAPPED)
S14        17   S10 NOT PY>2001
S15        17   S14 NOT PD>20011009
S16        14   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/Mar W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Feb
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Mar W3
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Mar W2
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/Mar W2
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Mar W1
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
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16/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03037509 E.I. Monthly No: EIM9103-011425
Title: Application issues in optical storage systems.
Author: Moller, Torben
Corporate Source: Litton Integrated Automation, Alameda, CA, USA
Conference Title: Storage and Retrieval Systems and Applications
Conference Location: Santa Clara, CA, USA Conference Date: 19900213
Sponsor: SPIE; Soc for Imaging Science and Technology
E.I. Conference No.: 13889
Source: Proceedings of SPIE - The International Society for Optical Engineering v 1248. Publ by Int Soc for Optical Engineering, Bellingham, WA, USA. p 142-146
Publication Year: 1990
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-0295-8
Language: English
Document Type: PA; (Conference Paper) Treatment: A; (Applications)
Journal Announcement: 9103
Abstract: A decision to implement an optical storage system raises a number of issues, some of which relate directly to the current capabilities of technology and some of which are operational. The determinants for success include a thorough analysis of existing operations, a clear requirements definition, and a careful **mapping** of the requirements to a configuration for the system. Although these steps are materially similar to the analysis required for any automation project, they have been less than well understood in the **context** of this **storage** technology. This paper will **identify** and discuss these tasks as they relate to the design of a complete system, using case studies to highlight the effects of work flows, storage algorithms, and communication requirements. In the process, the paper distills design experience in optical disk data management systems with hundreds of workstations and Terabytes of on-line storage. (Author abstract)
Descriptors: *DATA STORAGE, OPTICAL--*Disk; DATA PROCESSING
Identifiers: OPTICAL DISK DATA
Classification Codes:
741 (Optics & Optical Devices); 722 (Computer Hardware); 716 (Radar, Radio & TV Electronic Equipment); 723 (Computer Software)
74 (OPTICAL TECHNOLOGY); 72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

16/5/3 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01588158 ORDER NO: AAD97-37094
DESIGN AND DEVELOPMENT OF CELL QUEUING, PROCESSING, AND SCHEDULING MODULES FOR THE IPOINT INPUT-BUFFERED ATM TESTBED
Author: DUAN, HAORAN
Degree: PH.D.
Year: 1997
Corporate Source/Institution: UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN (0090)
Adviser: SUNG-MO KANG
Source: VOLUME 58/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3215. 319 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL ; PHYSICS, OPTICS
Descriptor Codes: 0544; 0752

This dissertation presents the concepts, principles, performance, and implementation of input queuing and cell-scheduling modules for the Illinois Pulsar-based Optical INTerconnect (iPOINT) input- **buffered** Asynchronous Transfer **Mode** (ATM) testbed.

Input queuing (IQ) ATM switches are well suited to meet the requirements of current and future ultra-broadband ATM networks. The IQ

structure imposes minimum memory bandwidth requirements for cell buffering, tolerates bursty traffic, and utilizes memory efficiently for multicast traffic. The lack of efficient cell queuing and scheduling solutions has been a major barrier to build high-performance, scalable IQ-based ATM switches. This dissertation proposes a new Three-Dimensional Queue (3DQ) and a novel Matrix Unit Cell Scheduler (MUCS) to remove this barrier.

3DQ uses a linked-list architecture based on Synchronous Random Access Memory (SRAM) to combine the individual advantages of per-virtual-circuit (per-VC) queuing, priority queuing, and N-destination queuing. It avoids Head of Line (HOL) blocking and provides per-VC Quality of Service (QoS) enforcement mechanisms. Computer simulation results **verify** the QoS capabilities of 3DQ. For multicast traffic, 3DQ provides efficient usage of cell buffering memory by storing multicast cells only once. Further, the multicast mechanism of 3DQ prevents a congested destination port from blocking other less-loaded ports. The 3DQ principle has been prototyped in the Illinois Input Queue (iiQueue) module. Using Field Programmable Gate Array (FPGA) devices, SRAM modules, and integrated on a Printed Circuit Board (PCB), iiQueue can process incoming traffic at 800 Mb/s. Using faster circuit technology, the same design is expected to operate at the OC-48 rate (2.5 Gb/s).

MUCS resolves the output contention by evaluating the weight index of each candidate and selecting the heaviest. It achieves near-optimal scheduling and has a very short response time. The algorithm originates from a heuristic strategy that leads to "socially optimal" solutions, yielding a maximum number of contention-free cells being scheduled. A novel mixed digital-analog circuit has been designed to implement the MUCS core functionality. The MUCS circuit **maps** the cell scheduling computation to the capacitor charging and discharging procedures that are conducted fully in parallel. The design has a uniform circuit structure, low interconnect counts, and low chip I/O counts. Using 2 μm CMOS technology, the design operates on a 100 MHz clock and finds a near-optimal solution within a linear processing time. The circuit has been **verified** at the transistor level by HSPICE simulation.

During this research, a five-port IQ-based optoelectronic iPOINT ATM switch has been developed and demonstrated. It has been fully functional with an aggregate throughput of 800 Mb/s. The second-generation IQ-based switch is currently under development. Equipped with iiQueue modules and MUCS module, the new switch system will deliver a multi-gigabit aggregate throughput, eliminate HOL blocking, provide per-VC QoS, and achieve near-100% link bandwidth utilization. Complete documentation of input modules and trunk module for the existing testbed, and complete documentation of 3DQ, iiQueue, and MUCS for the second-generation testbed are given in this dissertation.

16/5/5 (Item 4 from file: 35)

01261365 ORDER NO: AAD93-02340
IMPROVING LOCALITY AND PARALLELISM IN NESTED LOOPS
Author: WOLF, MICHAEL EDWARD
Degree: PH.D.
Year: 1992
Corporate Source/Institution: STANFORD UNIVERSITY (0212)
Adviser: MONICA S. LAM
Source: VOLUME 53/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4792. 225 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

Researchers have **identified** a core set of program transformations that are effective in array-based loop nest optimization: these loop transformations include interchange, skewing, reversal and tiling. Researchers have studied these transformations individually for their legality and effect on parallelism and memory hierarchy performance; but they have not discussed in any detail how to choose the combination of

transformations that best optimizes a loop nest. Other researchers have taken another approach: they consider each loop nest as a whole, applying an elegant matrix theory of loop nest transformation, but one that is only applicable to a limited class of loop nests, those whose dependences can be expressed as distance vectors. In this limited **context** , the problems of **memory** hierarchy improvement and parallelization are simplified, but their approach has not been extended to apply to general loop nests.

We have combined the elegance of the matrix theory with the generality of general dependence vectors into a new theory of loop transformation. This theory has enabled us to apply an algorithmic approach to solving optimization goals. Using this theory, we have developed efficient algorithms for the compiler to use to improve memory hierarchy utilization and parallelism of general loop nests. The parallelization improving algorithm maximizes the degree of parallelism within a loop nest, at either a coarse or fine granularity. The locality improving algorithm uses the same theory, and also reuse information about array accesses within loop nests, to guide the transformation process. The parallelization and locality improvement algorithms are unified so that locality and parallelism can be improved simultaneously without significantly reducing either.

We have implemented versions of these algorithms in Stanford's SUIF compiler and performed experimentation on the Perfect Club and the NASA kernels. We have found compiler locality improvement to significantly improve performance when applicable. We have also demonstrated a tremendous sensitivity of performance on tile size for tiled codes on machines with direct- **mapped** or low set associativity caches.

16/5/10 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

4108880 INSPEC Abstract Number: C9204-1180-045
Title: Linear programming and recurrent associative memories
Author(s): Kalaba, R.; Moon Kim; Moore, J.E., II
Author Affiliation: Univ. of Southern California, Los Angeles, CA, USA
Journal: International Journal of General Systems vol.20, no.2 p. 177-94
Publication Date: 1992 Country of Publication: UK
CODEN: IJGSD2 ISSN: 0308-1079
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Many optimization procedures presume the availability of an initial approximation in the neighborhood of a local or global optimum. Unfortunately, finding a set of good starting conditions is itself a nontrivial proposition. The authors describe a procedure for **identifying** approximate solutions to constrained optimization problems. Recurrent neural network structures are interpreted in the **context** of linear associative **memory** matrices. A recurrent associative memory (RAM) is trained to **map** the inputs of closely related transportation linear programs to optimal solution vectors. The procedure performs well when training cases are selected according to a simple rule, **identifying** good heuristic solutions for representation tests cases. Modest infeasibilities exist in some of these estimated solutions, but the basic variables associated with true optimums are usually apparent. In the great majority of cases, rounding **identifies** the true optimum. (18 Refs)
Subfile: C
Descriptors: content-addressable storage; linear programming; neural nets
Identifiers: linear programming; recurrent associative memories; approximate solutions; constrained optimization problems; neural network structures; linear associative memory matrices; heuristic solutions
Class Codes: C1180 (Optimisation techniques); C1230D (Neural nets)

16/5/11 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

02387156 INSPEC Abstract Number: C85010491

Title: Microcomputer-based synchronous multichannel data acquisition system

Author(s): Sridharan, G.

Author Affiliation: Defence Metall. Res. Lab., Hyderabad, India

Journal: IEEE Transactions on Industrial Electronics vol.IE-31, no.4 p.289-91

Publication Date: Nov. 1984 Country of Publication: USA

CODEN: ITIED6 ISSN: 0278-0046

U.S. Copyright Clearance Center Code: 0278-0046/84/1100-0289$01.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: Most multichannel data acquisition systems for digital measurements and control applications use a sequential data conversion method. Thus, the sampling instants of the analog signals are dispersed in time. However, synchronous sampling is desirable when the data are required for system **identification** studies, or when fast data conversion of a large number of analog channels is involved. A cost-effective technique is proposed for a microcomputer-based 8-channel synchronous data acquisition system. The software routine for complete data conversion and for storing the values in RAM takes only 93 mu s of CPU time when used with a single-board microcomputer SDK-85. Since the A/D converters (ADCs) are operated in a **memory - mapped mode** , the system can be expanded almost indefinitely. The circuit can handle ADCs of 12-bit resolution as well. (10 Refs)

Subfile: C

Descriptors: analogue-digital conversion; data acquisition

Identifiers: analogue digital convertors; SDK 85 microcomputer; synchronous multichannel data acquisition; sequential data conversion; sampling; analog signals; system **identification** ; RAM; CPU; ADCs

Class Codes: C3210G (Data acquisition systems); C5180 (A/D and D/A convertors); C5520 (Data acquisition equipment and techniques)

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Set     Items   Description
S1        396   TRANSLATION()(LOOKASIDE OR LOOK()ASIDE)()BUFFER?
S2     810153   CONTEXT OR CURRENT()STATUS OR CONDITION
S3     844672   VALID? OR AUTHENTICAT? OR VERIF? OR CERTIF?
S4     912475   MEMORY OR STORAGE OR CACHE? OR BUFFER?
S5          2   S1 AND S2 AND S3
S6         25   S1 AND S2
S7         25   S5 OR S6
S8         25   S7 NOT PY>2001
S9         25   S8 NOT PD>20011009
S10        18   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/Mar W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Feb
         (c) 2004 ProQuest Info&Learning
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File  65:Inside Conferences 1993-2004/Mar W3
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Mar W2
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/Mar W2
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Mar W1
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
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10/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05923172 E.I. No: EIP01385584311
Title: Towards virtually-addressed memory hierarchies
Author: Qiu, Xiaogang; Dubois, Michel
Corporate Source: Sun Microsystems Inc, Palo Alto, CA, United States
Conference Title: 7th International Symposium on High-Performance Computer Architecture
Conference Location: Nuevo Leon, Mex Conference Date: 20001020-20001024
Sponsor: IEEE
E.I. Conference No.: 57972
Source: IEEE High-Performance Computer Architecture Symposium Proceedings 2001.
Publication Year: 2001
CODEN: 85QSAT
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0110W4
Abstract: Currently cache hierarchies are indexed in parallel with a TLB but their tags are part of the physical address so that the memory hierarchy is physically addressed. This design faces problems as more concurrency is exploited in the processor core and as the memory demand of emerging applications is growing fast. The traditional TLB does not scale well inside the processor core and its hit rate can be poor for data-intensive applications or scientific applications without much locality. At the same time, given current trends towards computing in memory and in communication interfaces, virtual addresses are needed not just inside the processor but throughout the memory hierarchy. These observations have prompted us to revisit the problem of moving virtual address translation away from the processor. This paper introduces new ideas to enable the use of virtual addresses throughout the memory hierarchy. The major idea is the replacement of the TLB with a small Synonym Lookaside Buffer (SLB), which scales well because its size depends on the number of synonyms, and not on the size of the application or of the physical memory. We also characterize synonym usage, evaluate the amount of cache and SLB flushing due to remapping of addresses, and compare the miss rate of various virtual/physical cache organizations for several application domains. These evaluations show that virtually-addressed memory hierarchies overall have better performance behavior than physically-addressed memory hierarchies. Finally, we also show how virtually-addressed memory hierarchies facilitate natural, scalable multiprocessor extensions, as well as computing-in-memory in the **context** of general-purpose computers. (Author abstract) 42 Refs.
Descriptors: *Program processors; Storage allocation (computer); Buffer storage; Data storage equipment; Interfaces (computer); General purpose computers
Identifiers: Virtually-addressed memory hierarchies; Synonym Lookaside Buffers (SLB); **Translation lookaside buffers** (TLB)
Classification Codes:
723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 722.2 (Computer Peripheral Equipment)
723 (Computer Software, Data Handling & Applications); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

10/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05849245 E.I. No: EIP01276569886
Title: Online superpage promotion revisited
Author: Fang, Z.; Zhang, L.; Carter, J.; McKee, S.; Hsieh, W.
Corporate Source: Department of Computer Science University of Utah, Salt Lake City, UT, United States

Conference Title: Proceedings ACM SIGMETRICS 2000
Conference Location: Santa Clara, CA, United States Conference Date: 20000617-20000621
Sponsor: ACM SIGMETRICS
E.I. Conference No.: 58153
Source: Performance Evaluation Review v 28 n 1 2000. p 114-115
Publication Year: 2000
CODEN: PEREDN ISSN: 0163-5999
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0107W1
Abstract: Online superpage policies were evaluated in the **context** of the impulse memory controller. It was found that the presence of impulse changes the tradeoffs in choosing an appropriate policy and that the most aggressive policy becomes desirable. (Edited abstract) 4 Refs.
Descriptors: *Buffer storage; Online systems; Program translators; Cache memory; Algorithms
Identifiers: **Translation lookaside buffer** ; Online superpage promotion policies; Impulse memory controller
Classification Codes:
722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems)
722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

10/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05128301 E.I. No: EIP98104397124
Title: Wide address translation and protection for single address space operating systems
Author: Shieh, Shiuh-Pyng; Shyu, Ing-Jye; Shen, Chen-Yi
Corporate Source: Natl Chiao-Tung Univ, Hsinchu, Taiwan
Source: Proceedings of the National Science Council, Republic of China, Part A: Physical Science and Engineering v 22 n 5 Sep 1998. p 616-626
Publication Year: 1998
CODEN: PNAEE2 ISSN: 0255-6588
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9811W5
Abstract: In this paper, we present a new address translation and memory protection model to manage the wide 64-bit virtual address space, called the segment-based translation and protection (SBTP) model. It partitions a 64-bit virtual address space into 2**3**2 segments with equal size of 2**3**2 bytes. The SBTP model maintains a segment table to record used segments for each process. As a result of caching the per-process basis segment table on a designed memory cache, called the segment look-aside buffer (SLB), the virtual address translation time and protection rights **verification** time can be reduced. Furthermore, by separating the hardware mechanisms of address translation and protection, mapping information stored in the **translation look - aside buffer** (TLB) can be shared by all the processes and need not be flushed on each **context** switch. Thus, the cost of **context** switching compared with that conventional architectures is greatly reduced. Simulation results show that the proposed memory architecture effectively improves the performance of wide virtual address translation and memory protection for single address space operating systems. (Author abstract) 17 Refs.
Descriptors: *Computer operating systems; Computer architecture; Virtual storage; Buffer storage
Identifiers: Segment-based translation and protection (SBTP) model; Single address space operating systems; Virtual memory simulator; Wide address
Classification Codes:
722.1 (Data Storage, Equipment & Techniques)
722 (Computer Hardware); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING)

10/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05113945 E.I. No: EIP98094368415
Title: Options for dynamic address translation in COMAs
Author: Qiu, Xiaogang; Dubois, Michel
Corporate Source: Univ of Southern California, Los Angeles, CA, USA
Conference Title: Proceedings of the 1998 25th Annual International Symposium on Computer Architecture
Conference Location: Barcelona, Spain Conference Date: 19980627-19980701
Sponsor: IEEE; ACM SIGARCH
E.I. Conference No.: 48907
Source: Conference Proceedings - Annual International Symposium on Computer Architecture, ISCA 1998. IEEE Comp Soc, Los Alamitos, CA, USA. p 214-225
Publication Year: 1998
CODEN: CPAAEV ISSN: 0884-7495
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9811W1
Abstract: In modern processors, the dynamic translation of virtual addresses to support virtual memory is done before or in parallel with the first-level cache access. As processor technology improves at a rapid pace and the working sets of new applications grow insatiably the latency and bandwidth demands on the TLB (**Translation Lookaside Buffer**) are getting more and more difficult to meet. The situation is worse in multiprocessor systems, which run larger applications and are plagued by the TLB consistency problem. We evaluate and compare five options for virtual address translation in the **context** of COMAs (Cache Only Memory Architectures). The dynamic address translation mechanism can be located after the cache access provided the cache is virtual. In a particular design, which we call V-COMA for Virtual COMA, the physical address concept and the traditional TLB are eliminated. While still supporting virtual memory, V-COMA reduces the address translation overhead to a minimum. V-COMA scales well and works better in systems with large number of processors. As a machine running on virtual addresses, V-COMA provides a simple and consistent hardware model to the operating system and the compiler, in which further optimization opportunities are possible. (Author abstract) 33 Refs.
Descriptors: *Program processors; Virtual storage; Buffer storage; Multiprocessing systems; Computer hardware; Computer operating systems; Program compilers; Mathematical models; Optimization; Computer architecture
Identifiers: Dynamic address translation; Cache only memory architecture; **Translation lookaside buffer**
Classification Codes:
723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems); 921.6 (Numerical Methods); 921.5 (Optimization Techniques)
723 (Computer Software); 722 (Computer Hardware); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

10/5/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04871530 E.I. No: EIP97113930278
Title: Group contexts: An architectural approach to virtual sharing
Author: Mohamed, Ahmed; Sagahyroon, Assim
Corporate Source: Sun Microsystems, Mountain View, CA, USA
Conference Title: Proceedings of the 1997 6th IEEE Pacific Rim Conference

on Communications, Computers and Signal Processing. Part 1 (of 2)
Conference Location: Victoria, Can Conference Date: 19970820-19970822
Sponsor: IEEE
E.I. Conference No.: 47264
Source: IEEE Pacific RIM Conference on Communications, Computers, and Signal Processing - Proceedings v 1 1997. IEEE, Piscataway, NJ, USA,97CH36060. p 289-293
Publication Year: 1997
CODEN: 002121
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 9801W2
Abstract: Software managed **translation look - aside buffers** (TLBs) provide free grain address translations at a virtual page. This paper presents a novel scheme that exploits the aforementioned property to allow a group of processes to share system resources of write-protected memory segments. These resources consist of segment and address mapping data structures, and software translation cache and **translation look - aside buffer** entries. While this feature reduces allocation of kernel memory, it also better utilizes address translation caches by coalescing multiple entries into a single entry. The idea of virtual sharing is complicated by two issues. First, the virtual memory sub-system may not map shareable segments at the same virtual addresses and access permissions for all participants. We present a simple and flexible VM policy which enforces this requirement in the presence of dynamic linking and permission changes. Second, the underlying hardware address translation architecture may not explicitly support group sharing. In this work, we propose a Group **Context** TLB architecture which allows the system to share TLB entries of virtually shared pages. We also presents a judicious software multiplexing mechanism that enables the operating system to share software address translation mappings independent of the underlying hardware characteristics. (Author abstract) 11 Refs.
Descriptors: *Virtual storage; Buffer storage; Storage allocation (computer); Data structures; Computer architecture; Program translators; Computer operating systems; Computer software
Identifiers: Group **context translation look aside buffer** (TLB) architecture; Write protected memory segments; Hardware address translation architecture
Classification Codes:
722.1 (Data Storage, Equipment & Techniques); 723.2 (Data Processing); 723.1 (Computer Programming)
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

10/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04192273 E.I. No: EIP95062758005
Title: Software-controlled prefetching mechanism for software-managed TLBs
Author: Park, Jang Suk; Ahn, Gwang Seon
Corporate Source: Electronics and Telecommunications Research Inst, Taejon, S Korea
Source: Microprocessing and Microprogramming v 41 n 2 May 1995. p 121-136
Publication Year: 1995
CODEN: MMICDT ISSN: 0165-6074
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 9508W4
Abstract: The TLB (**Translation Lookaside Buffer**) miss services have been concealed from operating systems, but some new RISC architectures manage the TLB in software. Since software-managed TLBs provide flexibility to an operating system in page translation, they are considered an important factor in the design of microprocessors for open system environments. However, software-managed TLBs suffer from larger miss

penalty than hardware-managed TLBs, since they require more extra **context** switching overhead than hardware-managed TLBs. This paper introduces a new technique for reducing the miss penalty of software-managed TLBs by prefetching necessary TLB entries before being used. This technique is not inherently limited to specific applications. The key of this scheme is to perform the prefetch operations to update the TLB entries before first accesses so that TLB misses can be avoided. Using trace-driven simulation and a quantitative analysis, the proposed scheme is evaluated in terms of the miss rate and the total miss penalty. Our results show that the proposed scheme reduces the TLB miss rate by a factor of 6% to 77% due to TLB characteristics and page sizes. In addition, it is found that reducing the miss rate by the prefetching scheme reduces the total miss penalty and bus traffics in software-managed TLBs. (Author abstract) 21 Refs.

Descriptors: *Buffer storage; Computer software; Reduced instruction set computing; Computer operating systems; Computer simulation; Microcomputers; Virtual storage

Identifiers: **Translation lookaside buffer** ; Trace driven simulation; Prefetching

Classification Codes:

722.1 (Data Storage, Equipment & Techniques); 723.1 (Computer Programming); 723.5 (Computer Applications); 722.4 (Digital Computers & Systems)

722 (Computer Hardware); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING)

10/5/7 (Item 7 from file: 8)

03829265 E.I. No: EIP94031242985

Title: Simulation based study of TLB performance

Author: Chen, J. Bradley; Borg, Anita

Corporate Source: Carnegie Mellon Univ, Pittsburgh, PA, USA

Conference Title: Proceedings of the 19th Annual International Symposium on Compu- ter Architecture

Conference Date: 19920519-19920521

E.I. Conference No.: 19835

Source: Proceedings of the Ninth Annual International Symposium on Computer Architecture 1993. Publ by ACM, New York, NY, USA. p 114-123

Publication Year: 1993

ISBN: 0-89791-509-7

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical); A; (Applications)

Journal Announcement: 9405W2

Abstract: This paper presents the results of a simulation-based study of various **translation lookaside buffer** (TLB) architectures, in the **context** of a modern VLSI RISC processor. The simulators used address traces, generated by instrumented versions of the SPECmarks and several other programs running on a DECstation 5000. The performance of two-level TLBs and fully-associative TLBs were investigated. The amount of memory mapped was found to be the dominant factor in TLB performances. Small first-level FIFO instruction TLBs can be effective in two level TLB configurations. For some applications, the cycles-per-instruction (CPI) loss due to TLB misses can be reduced from as much as 5 CPI to negligible levels with typical TLB parameters through the use of variable-sized pages. (Author abstract) 12 Refs.

Descriptors: *Computer simulation; Computer architecture; Program processors; Computer systems programming; VLSI circuits

Identifiers: **Translation lookaside buffer** (TLB); Address traces; Cycles per instruction (CPI)

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits)

722 (Computer Hardware); 723 (Computer Software); 714 (Electronic Components)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

10/5/8 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02076721 E.I. Monthly No: EIM8603-014085
Title: OBJECT ORIENTED ARCHITECTURE.
Author: Dally, William J.; Kajiya, James T.
Corporate Source: California Inst of Technology, Pasadena, CA, USA
Conference Title: Conference Proceedings - 12th Annual International Symposium on Computer Architecture.
Conference Location: Boston, MA, USA Conference Date: 19850717
Sponsor: IEEE Computer Soc, Technical Committee on Architecture, Los Alamitos, CA, USA.; ACM, Special Interest Group on Architecture, New York, NY, USA.; IEEE, New York, NY, USA.
E.I. Conference No.: 07650
Source: Conference Proceedings - Annual Symposium on Computer Architecture 12th. Publ by IEEE, New York, NY, USA Available from IEEE Service Cent (Cat n 85CH2144-4), Piscataway, NJ, USA p 154-161
Publication Year: 1985
CODEN: CPAADU ISSN: 0149-7111 ISBN: 0-8186-0634-7
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8603
Abstract: A new machine architecture for high-performance execution of late-binding object-oriented languages is proposed. The two principal mechanisms for attaining this goal are a fast **context** allocation/access scheme and an instruction **translation lookaside buffer** . The concept and implementation of abstract instructions, using floating point addresses to solve the small-object problem, and a novel **context** allocation/access mechanism are discussed. 19 refs.
Descriptors: *COMPUTER ARCHITECTURE; COMPUTER PROGRAMMING LANGUAGES-- Problem Orientation
Identifiers: ALLOCATION/ACCESS SCHEMES; FLOATING POINT ADDRESSES
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

10/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01786344 E.I. Monthly No: EI8508065167 E.I. Yearly No: EI85029509
Title: DUAL PURPOSE USE OF TLB REGISTERS.
Author: Anon
Source: IBM Technical Disclosure Bulletin v 27 n 11 Apr 1985 p 6415
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8508
Abstract: This article describes the dual purpose use of **translation look - aside buffer** (TLB) registers that eliminate the need for an address register, which is normally used only to store the current address during an error **condition** . The TLB real registers are used as dual purpose registers.
Descriptors: *DATA STORAGE, DIGITAL
Identifiers: TLB REGISTERS; **TRANSLATION LOOK - ASIDE BUFFER** (TLB)
Classification Codes:
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

10/5/10 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7220203 INSPEC Abstract Number: C2002-04-6120-040

Title: Further cache and TLB investigation of the RAMpage memory hierarchy

Author(s): Machanick, P.; Patel, Z.

Author Affiliation: Sch. of Comput. Sci., Univ. of the Witwatersrand, Wits, South Africa

Conference Title: Hardware, Software and Peopleware. South African Institute of Computer Scientist and Information Technologists Annual Conference p.225

Editor(s): Renaud, K.; Kotze, P.; Barnard, A.

Publisher: Unisa Press, Pretoria, South Africa

Publication Date: 2001 Country of Publication: South Africa xix+226 pp.

ISBN: 1 86888 195 4 Material Identity Number: XX-2001-02851

Conference Title: Proceedings of SAICSIT 2001. South African Institute of Computer Science and Information Technology Annual Conference

Conference Date: 25-28 Sept. 2001 Conference Location: Pretoria, South Africa

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Summary form only given. The RAMpage memory hierarchy is an alternative to the traditional division between cache and main memory: main memory is moved up a level and DRAM is used as a paging device. Earlier RAMpage work has shown that the RAMpage model scales up better with the growing CPU-DRAM speed gap, especially when **context** switches are taken on misses. This paper investigates the effect of more aggressive first-level (L1) cache and **translation lookaside buffer** (TLB) implementations, with other parameters kept the same as in previous work, to illustrate that a more aggressive design improves the competitiveness of RAMpage. The more aggressive L1 shows an increase in the advantage of RAMpage with **context** switches on misses, supporting the hypothesis that a more aggressive L1 favours RAMpage. However, results without **context** switches on misses are less conclusive. A larger TLB, as predicted, makes RAMpage viable over a wider range of page sizes.

Subfile: C

Descriptors: cache storage; paged storage; random-access storage

Identifiers: RAMpage memory hierarchy; cache investigation; TLB investigation; main memory; DRAM; paging device; CPU-DRAM speed; **context** switches; first-level cache; **translation lookaside buffer** ; page sizes

Class Codes: C6120 (File organisation); C5320 (Digital storage)

10/5/11 (Item 2 from file: 2)

6655693 INSPEC Abstract Number: C2000-09-6120-004

Title: Online superpage promotion revisited

Author(s): Zhen Fang; Lixin Zhang; Carter, J.; McKee, S.; Hsieh, W.

Author Affiliation: Dept. of Comput. Sci., Utah Univ., Salt Lake City, UT, USA

Journal: Performance Evaluation Review Conference Title: Perform. Eval. Rev. (USA) vol.28, no.1 p.114-15

Publisher: ACM,

Publication Date: June 2000 Country of Publication: USA

CODEN: PEREDN ISSN: 0163-5999

SICI: 0163-5999(200006)28:1L.114:OSPR;1-S

Material Identity Number: P301-2000-003

Conference Title: ACM SIGMETRICS '2000. International Conference on Measurement and Modeling of Computer Systems

Conference Sponsor: ACM

Conference Date: 17-21 June 2000 Conference Location: Santa Clara, CA, USA

Language: English Document Type: Conference Paper (PA); Journal Paper (JP)

Treatment: Practical (P)
Abstract: The amount of data that a typical **translation lookaside buffer** (TLB) can map has not kept pace with the growth in cache sizes and application footprints. As a result, the cost of handling TLB misses limits the performance of an increasing number of applications. The use of superpages, multiple adjacent virtual memory pages that can be mapped with a single TLB entry, extends a TLB's reach without significantly increasing its size or cost. Previous studies have shown that simple online policies that decide to create superpages dynamically can be effective in reducing TLB penalties. We reevaluate online superpage policies in the **context** of the impulse memory controller, which supports no-copy superpage construction. Our results show that the presence of impulse changes the tradeoffs in choosing an appropriate policy, and that the most aggressive policy becomes desirable. (4 Refs)
Subfile: C
Descriptors: memory architecture; paged storage; performance evaluation; table lookup
Identifiers: online superpage; **translation lookaside buffer** ; superpages; multiple adjacent virtual memory pages; impulse memory controller
Class Codes: C6120 (File organisation); C5470 (Performance evaluation and testing)

10/5/12 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6302011 INSPEC Abstract Number: C1999-09-6150G-001
Title: Design and implementation of a performance measurement tool for a microkernel-based operating system
Author(s): Moon-Seok Chang; Kern Koh; Joon-Won Lee; Hae-Jin Kim
Journal: Journal of KISS(C) (Computing Practices) vol.5, no.2 p. 236-46
Publisher: Korea Inf. Sci. Soc,
Publication Date: April 1999 Country of Publication: South Korea
CODEN: CKNCFY ISSN: 1226-2293
SICI: 1226-2293(199904)5:2L.236:DIPM;1-4
Material Identity Number: E347-1999-004
Language: Korean Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: A recent trend in operating system development is microkernel design. Microkernels require a newly designed tool for performance analysis and tuning, since they have a different structure compared to the monolithic ones. In this paper, we present MKperf, a performance tool for a microkernel-based operating system. MKperf has the capability to monitor **context** switches and remote procedure calls, which are important activities for the performance of a microkernel. In addition, this tool monitors various hardware events that are critical to the performance of memory systems, including caches and TLBs (**translation lookaside buffers**). As a result, MKperf provides useful information for the performance analysis of microkernel-based operating systems. (16 Refs)
Subfile: C
Descriptors: operating system kernels; remote procedure calls; software performance evaluation; software tools; system monitoring; tuning
Identifiers: performance measurement tool; microkernel-based operating system; performance analysis; performance tuning; MKperf; **context** switch monitoring; remote procedure call monitoring; hardware event monitoring; memory systems; caches; **translation lookaside buffers**
Class Codes: C6150G (Diagnostic, testing, debugging and evaluating systems); C6115 (Programming support); C6150J (Operating systems)

10/5/13 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6074746 INSPEC Abstract Number: C9812-6120-023

Title: Wide address translation and protection for single address space operating systems

Author(s): Shiuh-Pyng Shieh; Ing-Jye Shyu; Chen-Yi Shen

Author Affiliation: Inst. of Comput. Sci. & Inf. Eng., Nat. Chiao Tung Univ., Hsinchu, Taiwan

Journal: Proceedings of the National Science Council, Republic of China, Part A (Physical Science and Engineering) vol.22, no.5 p.616-25

Publisher: Natl. Sci. Council, Taiwan,

Publication Date: Sept. 1998 Country of Publication: Taiwan

CODEN: PNAEE2 ISSN: 0255-6588

SICI: 0255-6588(199809)22:5L.616:WATP;1-X

Material Identity Number: P858-98005

U.S. Copyright Clearance Center Code: 0255-6588/98/$5.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Experimental (X)

Abstract: In this paper, we present a new address translation and memory protection model to manage the wide 64-bit virtual address space, called the segment-based translation and protection (SBTP) model. It partitions a 64-bit virtual address space into 2/sup 32/ segments with equal size of 2/sup 32/ bytes. The SBTP model maintains a segment table to record used segments for each process. As a result of caching the per-process basis segment table on a designed memory cache, called the segment look-aside buffer (SLB), the virtual address translation time and protection rights **verification** time can be reduced. Furthermore, by separating the hardware mechanisms of address translation and protection, mapping information stored in the **translation look - aside buffer** (TLB) can be shared by all the processes and need not be flushed on each **context** switch. Thus, the cost of **context** switching compared with that conventional architectures is greatly reduced. Simulation results show that the proposed memory architecture effectively improves the performance of wide virtual address translation and memory protection for single address space operating systems. (17 Refs)

Subfile: C

Descriptors: memory architecture; operating systems (computers); performance evaluation; storage allocation; virtual storage

Identifiers: wide address translation; memory protection model; single address space operating systems; virtual address space; segment-based translation and protection model; segment table; memory cache; segment look-aside buffer; mapping information; memory architecture; **context** switching

Class Codes: C6120 (File organisation); C6150J (Operating systems); C5310 (Storage system design); C5470 (Performance evaluation and testing)

10/5/14 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

5985661 INSPEC Abstract Number: C9809-6120-022

Title: Options for dynamic address translation in COMAs

Author(s): Xiaogang Qiu; Dubois, M.

Author Affiliation: Dept. of Electr. Eng., Univ. of Southern California, Los Angeles, CA, USA

Conference Title: Proceedings. 25th Annual International Symposium on Computer Architecture (Cat. No.98CB36235) p.214-25

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1998 Country of Publication: USA xiii+394 pp.

ISBN: 0 8186 8491 7 Material Identity Number: XX98-01756

U.S. Copyright Clearance Center Code: 1063-6897/98/$10.00

Conference Title: Proceedings of ISCA 98: International Symposium on Computer Architecture

Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Archit.; ACM SIGARCH; Comision Interministerial de Ciencia y Tecnol. (CICYT);

Comissio Interdept. Recerca i Innovacio Tecnol. (CIRIT); Univ. Politech. Catalunya (UPC)
Conference Date: 27 June-1 July 1998 Conference Location: Barcelona, Spain
Language: English Document Type: Conference Paper (PA).
Treatment: Applications (A); Practical (P)
Abstract: In modern processors, the dynamic translation of virtual addresses to support virtual memory is done before or in parallel with the first-level cache access. As processor technology improves at a rapid pace and the working sets of new applications grow insatiably the latency and bandwidth demands on the TLB (**Translation Lookaside Buffer**) are getting more and more difficult to meet. The situation is worse in multiprocessor systems, which run larger applications and are plagued by the TLB consistency problem. We evaluate and compare five options for virtual address translation in the **context** of COMAs (Cache Only Memory Architectures). The dynamic address translation mechanism can be located after the cache access provided the cache is virtual. In a particular design, which we call V-COMA for Virtual COMA, the physical address concept and the traditional TLB are eliminated. While still supporting virtual memory, V-COMA reduces the address translation overhead to a minimum. V-COMA scales well and works better in systems with large number of processors. As a machine running on virtual addresses, V-COMA provides a simple and consistent hardware model to the operating system and the compiler, in which further optimization opportunities are possible. (33 Refs)
Subfile: C
Descriptors: cache storage; memory architecture; virtual storage
Identifiers: dynamic address translation; virtual addresses; virtual memory; first-level cache access; processor technology; **translation lookaside buffer** ; cache only memory architectures; Virtual COMA
Class Codes: C6120 (File organisation); C5310 (Storage system design)

10/5/15 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

4974916 INSPEC Abstract Number: C9508-6150C-001
Title: A software-controlled prefetching mechanism for software-managed TLBs
Author(s): Jang Suk Park; Gwang Seon Ahn
Author Affiliation: Comput. Res. Dept., Electron. & Telecommun. Res. Inst., Taejon, South Korea
Journal: Microprocessing & Microprogramming vol.41, no.2 p.121-36
Publication Date: May 1995 Country of Publication: Netherlands
CODEN: MMICDT ISSN: 0165-6074
U.S. Copyright Clearance Center Code: 0165-6074/95/$09.50
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The TLB (**Translation Lookaside Buffer**) miss services have been concealed from operating systems, but some new RISC architectures manage the TLB in software. Since software-managed TLBs provide flexibility to an operating system in page translation, they are considered an important factor in the design of microprocessors for open system environments. However, software-managed TLBs suffer from larger miss penalty than hardware-managed TLBs, since they require more extra **context** switching overhead than hardware-managed TLBs. This paper introduces a new technique for reducing the miss penalty of software-managed TLBs by prefetching necessary TLB entries before being used. This technique is not inherently limited to specific applications. The key of this scheme is to perform the prefetch operations to update the TLB entries before first accesses so that TLB misses can be avoided. Using trace-driven simulation and a quantitative analysis, the proposed scheme is evaluated in terms of the miss rate and the total miss penalty. Our results show that the proposed scheme reduces the TLB miss rate by a factor of 6% to 77% due to TLB characteristics and page sizes. In addition, it is found that reducing

the miss rate by the prefetching scheme reduces the total miss penalty and bus traffics in software-managed TLBs. (21 Refs)
Subfile: C
Descriptors: discrete event simulation; operating systems (computers); program interpreters
Identifiers: software-controlled prefetching mechanism; software-managed TLBs; **translation lookaside buffer** ; operating systems; RISC architectures; page translation; microprocessors; open system environments; **context** switching overhead; trace-driven simulation; quantitative analysis; prefetching scheme
Class Codes: C6150C (Compilers, interpreters and other processors); C6150J (Operating systems); C6185 (Simulation techniques)

10/5/16 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

4669559 INSPEC Abstract Number: B9406-1265F-066, C9406-5130-030
Title: 88110: memory system and bus interface
Author(s): Arends, J.
Author Affiliation: Motorola Inc., Austin, TX, USA
p.189-92
Editor(s): Juj, H.; Moser, A.T.
Publisher: Electron. Conventions Manage, Ventura, CA, USA
Publication Date: 1992 Country of Publication: USA vii+366 pp.
Conference Title: Proceedings of NORTHCON '92
Conference Sponsor: IEEE; ERA; Electron. Manuf. Assoc
Conference Date: 19-21 Oct. 1992 Conference Location: Seattle, WA, USA
Availability: Western Periodicals, 424 East Main Street, Ventura, CA 93001, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The Motorola 88110 symmetric superscalar microprocessor's memory system and bus interface unit is composed of an 8 KByte instruction cache, an 8 KByte data cache, independent instruction and data **translation lookaside buffers** , and a bus interface unit that will handle split bus transactions. The memory system and bus interface have been optimized for high hit rates, fast **context** switching, reduced bus traffic, and high bandwidth. The 88110 also provides flexibility in address translations and hardware multiprocessor features. (2 Refs)
Subfile: B C
Descriptors: buffer storage; microprocessor chips; system buses
Identifiers: symmetric superscalar microprocessor; Motorola 88110; memory system; bus interface unit; instruction cache; data cache; lookaside buffers; split bus transactions; hit rates; **context** switching; bus traffic; bandwidth; address translations; 8 KB
Class Codes: B1265F (Microprocessors and microcomputers); C5130 (Microprocessor chips); C5320G (Semiconductor storage); C5610S (System buses)
Numerical Indexing: memory size 8.2E+03 Byte

10/5/17 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

4508468 INSPEC Abstract Number: C9312-6120-009
Title: Fast inter-object communication using slotted virtual space
Author(s): Mitsuzawa, A.; Yokote, Y.; Tokoro, M.
Author Affiliation: Dept. of Comput. Sci., Keio Univ., Tokyo, Japan
Journal: Transactions of the Information Processing Society of Japan vol.34, no.5 p.994-1009
Publication Date: May 1993 Country of Publication: Japan
CODEN: JSGRD5 ISSN: 0387-5806
Language: Japanese Document Type: Journal Paper (JP)

Treatment: Practical (P)
Abstract: The slotted virtual memory management scheme which enhances performance of inter-object communication within the same machine in operating systems is proposed. It divides a virtual space into equal sized fragments, called slots, and gives each object one or more slots. It enables the following techniques: **context** -switches and flushes of both **translation lookaside buffer** (TLB) entries and cache entries, become unnecessary, by placing several objects into the same space; frequencies of communication between virtual spaces can be reduced by moving objects dynamically; the execution of extra paths can be avoided by replacing them with local procedure calls. Measures on the Apertos operating system are carried out. (15 Refs)
Subfile: C
Descriptors: buffer storage; operating systems (computers); virtual storage
Identifiers: fast inter-object communication; slotted virtual space; slotted virtual memory management scheme; operating systems; **context** -switches; flushes; **translation lookaside buffer** ; cache entries; TLB; local procedure calls; Apertos operating system
Class Codes: C6120 (File organisation); C6150J (Operating systems)

10/5/18 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00726505 I93104189259
Titel japanisch
(Schnelle Kommunikation zwischen Objekten mit Hilfe virtueller Speicherschlitze)
(Fast inter-object communication using slotted virtual space)
Mitsuzawa, A; Yokote, Y; Tokoro, M
Dept. of Comput. Sci., Keio Univ., Tokyo, Japan
Transactions of Information Processing Society of Japan, v34, n5, pp994-1009, 1993
Document type: journal article Language: Japanese
Record type: Abstract

ABSTRACT:
The slotted virtual memory management scheme which enhances performance of inter-object communication within the same machine in operating systems is proposed. It divides a virtual space into equal sized fragments, called slots, and gives each object one or more slots. It enables the following techniques: **context** -switches and flushes of both **translation lookaside buffer** (TLB) entries and cache entries, become unnecessary, by placing several objects into the same space; frequencies of communication between virtual spaces can be reduced by moving objects dynamically; the execution of extra paths can be avoided by replacing them with local procedure calls. Measures on the Apertos operating system are carried out.

DESCRIPTORS: BUFFER STORAGE; OPERATING SYSTEM--COMPUTERS; VIRTUAL MEMORY; DATA COMMUNICATION; OBJECT ORIENTED PROGRAMMING; MEMORY MANAGEMENT; CACHE MEMORIES
IDENTIFIERS: OPERATING SYSTEMS; FAST INTER OBJECT COMMUNICATION; SLOTTED VIRTUAL SPACE; SLOTTED VIRTUAL MEMORY MANAGEMENT SCHEME; **CONTEXT** SWITCHES ; FLUSHES; **TRANSLATION LOOKASIDE BUFFER** ; CACHE ENTRIES; TLB; LOCAL PROCEDURE CALLS; APERTOS OPERATING SYSTEM; Betriebssystem; Objektkommunikation

```
Set     Items   Description
S1     380624   (TRANSLATION OR TABLE)()(LOOKASIDE OR LOOK()ASIDE)()BUFFER?
              OR TLB OR MAP OR MAPPING OR MAPS OR MAPPED
S2     960707   CONTEXT OR CURRENT()STATUS OR CONDITION OR MODE
S3    2595734   VALID? OR AUTHENTICAT? OR VERIF? OR CERTIF? OR IDENTIF?
S4    1382265   MEMORY OR STORAGE OR CACHE? OR BUFFER?
S5       1120   S1 (S) S2 (S) S3
S6       6357   S2 (3N) S4
S7        253   S1 (S) S6
S8       4064   S3 (2N) (FLAG? OR INDICATOR? OR POINTER?)
S9          0   S7 (S) S8
S10        17   S7 (S) S3
S11         0   S5 (S) (DEMAPPING OR DEMAP OR DEMAPS OR DEMAPPED)
S12        16   S10 NOT PY>2001
S13        15   S12 NOT PD>20011009
S14        13   RD (unique items)
S15       650   TRANSLATION()(LOOKASIDE OR LOOK()ASIDE)()BUFFER?
S16        27   S15 (S) S2
S17         1   S16 (S) S3
S18        27   S16 OR S17
S19        22   S18 NOT PY>2001
S20        22   S19 NOT PD>20011009
S21        20   RD (unique items)
S22        20   S21 NOT S14
File  15:ABI/Inform(R) 1971-2004/Mar 20
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/Mar W2
         (c) 2004 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2004/Mar 22
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/Mar W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Mar 22
         (c) 2004 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2004/Mar 22
         (c) 2004 McGraw-Hill Co. Inc
File 636:Gale Group Newsletter DB(TM) 1987-2004/Mar 22
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Mar 22
         (c) 2004 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2004/Mar 22
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Feb
         (c) 2004 The HW Wilson Co
```

22/3,K/1 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01030917 96-80310
A software-controlled prefetching mechanism for software-managed TLBs
Park, Jang Suk; Ahn, Gwang Seon
Microprocessing & Microprogramming v41n2 PP: 121-136 May 1995
ISSN: 0165-6074 JRNL CODE: EUJ

ABSTRACT: The **translation lookaside buffer** (TLB) miss services have been concealed from operating systems, but some new RISC architectures manage the TLB...

... software-managed TLBs suffer from larger miss penalty than hardware-managed TLBs, since they require more extra **context** switching overhead than hardware-managed TLBs. A new technique is introduced for reducing the miss penalty of...

22/3,K/2 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00681105 93-30326
Alpha AXP architecture
Sites, Richard L
Communications of the ACM v36n2 PP: 33-44 Feb 1993
ISSN: 0001-0782 JRNL CODE: ACM
WORD COUNT: 7830

...TEXT: includes a Processor Status (PS) word, Kernel and User stack pointers, a Process Control Block base for **context** switching, a Process-unique value for threads, and a processor number for multiprocessor dispatching. Additional PALcode states may include floating-point enable bit, interrupt priority level, and **translation lookaside buffers** for mapping instruction-stream and data-stream virtual addresses. All this state is soft, in the sense...

22/3,K/3 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00533320 CMP ACCESSION NUMBER: EET19930524S3608
29200s tweaked for 3V/5V
ELECTRONIC ENGINEERING TIMES, 1993, n 747, 60
PUBLICATION DATE: 930524
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design - Solid State
WORD COUNT: 347

... cache and 2-kbyte data cache; a single-cycle 32-bit multiplier; a 16-entry MMU with **translation lookaside buffer** , and support for four banks of ROM with 8-, 16- and 32-bit interfaces, as well as...

...first member of the 29000 family to offer four-channel DMA support, with a fly-by operation **mode** to allow speeds in excess of 2,000 Mbytes/second in the DMA channel.
For the low...

22/3,K/4 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01830978 SUPPLIER NUMBER: 17270061 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Patent Watch.
Belgard, Rich
Microprocessor Report, v9, n11, p25(1)
August 21, 1995
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 759 LINE COUNT: 00060

TEXT:
...a cache for the desired instruction. On a slow path to main memory is a large main **translation lookaside buffer** (TLB) that holds address translations. On a fast path is a smaller translation write buffer (TWB), a ...

...the contents of the cache for a hit. The guess access is allowed to proceed upon the **condition** that there is a hit in the TWB (the TWB is able to translate the logical address...

...a physical address) and a miss in the 1-cache. The guess access is canceled upon the **condition** that there is either a miss in the TWB (the TWB is unable to translate the logical...

22/3,K/5 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01772891 SUPPLIER NUMBER: 16811984 (USE FORMAT 7 OR 9 FOR FULL TEXT)
HP showing architecture for 64-bit PA-RISC MPU. (HP developing PA-8000 PA-RISC microprocessor)
DeTar, Jim
Electronic News (1991), v41, n2055, p66(2)
March 6, 1995
ISSN: 1061-6624 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 777 LINE COUNT: 00062

... fetches up to four quadword-aligned instructions per cycle, a large (56-entry) reorder buffer, branch prediction **mode** , an address reorder buffer (ARB) to the dual-ported/single-level off-chip data cache, 96-entry **translation lookaside buffer** (TLB), and support for up to eight-way multiprocessing without any external glue logic.
In what could...

22/3,K/6 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01674558 SUPPLIER NUMBER: 15091801 (USE FORMAT 7 OR 9 FOR FULL TEXT)
VME modules SPARC performance race. (Force Computers and Themis Computer battle in the SPARC-based Sun-compatible VME market)
Andrews, Warren
Computer Design, v33, n3, p46(3)
March, 1994
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1668 LINE COUNT: 00132

... translation from 32-bit virtual address to the 36-bit physical address called for by MBus. A **context** register is used to **identify** up to 65,000 contexts. A **translation look - aside buffer** (TLB) completes address translation and improves the MMU's translation performance. The TLB supports 64 entries as...

22/3,K/7 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01636463 SUPPLIER NUMBER: 14412680 (USE FORMAT 7 OR 9 FOR FULL TEXT)
RISC vs. CISC for realtime: a software perspective. (reduced-instruction-set computer processors, complex-instruction-set computer processors) (Special Report: RISC in realtime) (Tutorial)
Talbot, James W.
Computer Design, v32, n8, p74(3)
August, 1993
DOCUMENT TYPE: Tutorial ISSN: 0010-4566 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2208 LINE COUNT: 00185

... hence in realtime systems. Determinism and throughput may be adversely affected by table walks, page faults and **context** switches. **Translation look - aside buffers** that are lockable can restore determinism and performance.
* Pipelines and instruction units. Depending on the implementation, a ...

22/3,K/8 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01531026 SUPPLIER NUMBER: 12475720 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Design verification of the HP 9000 Series 700 PA-RISC workstations. (includes related articles on HP's standard PA-RISC test programs, simulation tools used for testing, debugging tools and metrics) (Technical)
Ahi, Ali M.; Burroughs, Gregory D.; Gore, Audrey B.; LaMar, Steve W.; Lin, Chi-Yen R.; Wiemann, Alan L.
Hewlett-Packard Journal, v43, n4, p34(9)
August, 1992
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 5819 LINE COUNT: 00459

... a program, the initialization code sets up the system resources (control registers, general registers, floating-point registers, **translation lookaside buffers** or TLBs, etc.) to certain states. The initialization code runs in real **mode** . It turns on the virtual **mode** before execution switches to the random code. The necessary setup for virtual addressing **mode** includes TLB entries, address queues, the processor status word, and so on. The switch from real to virtual **mode** takes place on the last instruction in the initialization code. Once in virtual **mode** , execution of instructions on the random code page continues indefinitely until a recovery counter trap occurs.
BPS...

22/3,K/9 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01301106 SUPPLIER NUMBER: 07466446 (USE FORMAT 7 OR 9 FOR FULL TEXT)
National Advanced ships partitioning early, improves ESA. (Multiple Logical Processor Facility for AS/EX main frames) (Enterprise Systems Architecture)
Computergram International, n1231, CGI07310002
July 31, 1989
ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 202 LINE COUNT: 00016

... enhanced its forthcoming implementation of IBM's Enterprise Systems Architecture with proprietary hardware accelerators for Access Register **Mode** , optimised to reduce the time needed to translate data addresses

using access registers for access to ESA data spaces. The AS/EX machines also use access register **translation lookaside buffers** to imp rove performance, with storage of up to 256 recently-used addresses. Enterprise Systems Architecture support...

22/3,K/10 (Item 7 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01288597 SUPPLIER NUMBER: 07060390 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The Clipper (TM) Processor: instruction set architectures and implementation. (product announcement) (technical)
Hollingsworth, Walter; Sachs, Howard; Smith, Alan Jay
Communications of the ACM, v32, n2, p200(20)
Feb, 1989
DOCUMENT TYPE: technical ISSN: 0001-0782 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 9556 LINE COUNT: 00758

The CLIPPER microprocessor uses caching and virtual memory as the standard **mode** of operation. The associated CAMMU chips each contain a 4 Kbyte cache, a **translation lookaside buffer** (TLB), and a translator. One CAMMU is used for instruction references and the other for data; the...

22/3,K/11 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01245079 SUPPLIER NUMBER: 06211344 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Two that tango on the 80386. (DOS-under-UNIX systems)
Sarno, Kenneth M.
UNIX Review, v6, n1, p64(9)
Jan, 1988
ISSN: 0742-3136 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6942 LINE COUNT: 00530

... are 16-bit modes whose only purpose is to provide for backward compatibility.
In "32-bit protected **mode** ", the 80386 is a much more powerful device than any of its Intel predecessors. At 32 bits...

...address space. The paging hardware needed to manage these large virtual spaces is on-chip, including a **translation look - aside buffer** that caches the most recently used page table entries to achieve added performance. As a result of these and other enhancements, the 32-bit **mode** of the 80386 is well able to support UNIX and other demanding operating systems.
The other three...

22/3,K/12 (Item 9 from file: 275)
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01243657 SUPPLIER NUMBER: 06307201 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Designers seek new approaches to open I-O bottlenecks. (Special Report on I-O Bottlenecks)
Wilson, Ron
Computer Design, v27, n2, p57(11)
Jan 15, 1988
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6528 LINE COUNT: 00510

... on-chip design efforts on making bus cycles efficient, rather than on implementing a cache or burst- **mode** controller. "We designed a

pipelined address **mode** for the 80386 that makes address and control signals available before the end of the preceeding bus...

...states, letting the CPU run faster. Also, the chip's prefetch queue and the memory manager's **translation lookaside buffer** tend to cut down on bus loading. As a result, about one-half of our customers running...

22/3,K/13 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01233314 SUPPLIER NUMBER: 06588513
MIPS team to field faster RISC chip set. (MIPS Computer Systems)
Rogers, Kathy
Electronic Engineering Times, n481, p53(2)
April 11, 1988
ISSN: 0192-1541 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

...ABSTRACT: Mips. The microprocessor has a MMU, a cache controller, 512 Kbytes of instruction and data caches, a **translation look - aside buffer** , and a floating point coprocessor interface. the floating point coprocessor is the R3010 which supports IEEE standard...

...buffer allows the processor to do write operations during run cycles. All of the chips have a **mode** pin which, when activated, causes them to function like the previous generation R2000 devices.

22/3,K/14 (Item 11 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01204883 SUPPLIER NUMBER: 06041883 (USE FORMAT 7 OR 9 FOR FULL TEXT)
One chip MMU-cache gives boost to CPU hit rate.
LaRocca, Frank D.; Padnos, Steve; Hayes, Norm
Electronic Design, v35, p115(4)
Oct 15, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2034 LINE COUNT: 00157

... accommodate one or more users demanding multiuser-multitasking capability for business and engineering applications.
In a standalone **mode** with the WE 32200 microprocessor, the memory-management cache unit typically supplies a 99.6% hit rate in the descriptor cache, or **translation lookaside buffer** (TLB), and 80% to 85% hit rate in the data cache. The hit rate is the probability...

22/3,K/15 (Item 12 from file: 275)
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01204305 SUPPLIER NUMBER: 04635102 (USE FORMAT 7 OR 9 FOR FULL TEXT)
32-bit microprocessors. (1987 technology forecast)
Bursky, Dave
Electronic Design, v35, p128(8)
Jan 8, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4367 LINE COUNT: 00333

... It can rapidly translate to physical addresses by means of an on-chip, 64-entry fully associative **translation look - aside buffer** that accesses dual 8-kbyte data and instruction caches.
Along the same lines, MIPS plans to add...

22/3,K/16 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

01263364 Supplier Number: 41358356 (USE FORMAT 7 FOR FULLTEXT)
SPARC in Embedded Applications
RISC Management, n20, pN/A
June, 1990
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1661

... the cache control register. This chip also has the ability to lock page descriptors in the MMU **translation look - aside buffer** , which might otherwise be flushed during a **context** switch.
Embedded Application Development Tools
The success of RISC processors in embedded applications will depend greatly on...

22/3,K/17 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03783154 Supplier Number: 45383721 (USE FORMAT 7 FOR FULLTEXT)
HP Showing Architecture For 64-Bit PA-RISC MPU
Electronic News (1991), p66
March 6, 1995
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 707

... fetches up to four quadword-aligned instructions per cycle, a large (56-entry) reorder buffer, branch prediction **mode** , an address reorder buffer (ARB) to the dual -ported/single-level off-chip data cache, 96-entry **translation lookaside buffer** (TLB), and support for up to eight-way multiprocessing without any external glue logic.
In what could...

22/3,K/18 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03196372 Supplier Number: 44377503 (USE FORMAT 7 FOR FULLTEXT)
The art of configuring a custom design
Electronic Engineering Times, p40
Jan 24, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1275

... support the MIPS Instruction Set Architecture (ISA).
To support efficient embedded applications, HDL started by removing the **Translation Lookaside Buffer** (TLB). HDL estimates that removing the TLB and all co-processor zero registers, which supported the memory...

...embedded applications, HDL also implemented the MR300 as a physical address space processor, retaining User- and Kernel- **mode** memory protection and providing access to the full 4-Gbyte address space.
HDL has extensively redesigned the...

22/3,K/19 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03006261 Supplier Number: 44080515 (USE FORMAT 7 FOR FULLTEXT)
Fujitsu offers 20- and 40-MHz Sparclites
Electronic Engineering Times, pP16
Sept 6, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 195

... associative 8-kbyte instruction cache and a 2-kbyte data cache, as well as support for burst **mode** (required in high-performance memory systems). A **translation lookaside buffer** permits caching of the most recent translations.

The central integer unit uses a five-stage pipeline that...

22/3,K/20 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01848645
Simulation in the design of the Am29000 microprocessor
Electronic Engineering November, 1987 p. 44-52
ISSN: 0013-4902

... instruction buses), on-chip branch target chache for caching up to 32 jump targets, an on-chip **translation lookaside buffer** to demand paged memory scheme, and a register file that can be used as a stack cache ...

... the specific instruction of the user. The bus interface unit is capable of getting instructions in burst **mode** so that once the latency of a nonsequential fetch is over the processor can once again maintain...